

Edge Effects on the TSV Array Capacitances and their Performance Influence

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Abstract

The TSV capacitances are essential to estimate the pattern dependent performance of 3-D interconnects. A full-chip capacitance extraction with a field solver is very cost intensive and therefore not suitable for a fast design exploration. An accurate and scalable high-level TSV capacitance model is required. However, the previously used model does not include the edge effects, which can influence the capacitance values by magnitudes. In a quadratic 36 bit array, 20 TSVs are located at the edges. Therefore, the capacitance model needs to be extended by the edge effects, which is the main contribution of this work. The experimental results of this paper show that for 48 different modern TSV structures, the presented model reduces the root-mean-square-error (RMSE) by over 95 %, compared to the previously used model. For the estimation of the pattern dependent TSV array energy consumption, the experimental results reveal a normalized RMSE of 4.50 % for the presented model, while the previously used model shows a RMSE of 41.62 %. Additionally, a case study is presented which proves that existing TSV coding approaches, derived by means of the previous model, are impractical due to the edge effects.

Keywords: Through-silicon-via, coding, capacitance model, performance estimation, 3-D integration

1. Introduction

A promising solution to overcome the interconnect problem is the integration into the third dimension [1], as it reduces the average interconnect length. Furthermore, a 3-D system-on-chip (3-D SoC) enables a heterogeneous integration and a reduction of the overall system footprint. The interconnect structure between the dies of a 3-D SoC typically consists of through silicon vias (TSVs), as they yield to a high reliability. TSVs are usually bundled together rather than used in isolation [2]. By using regular TSV arrays, it is possible to generate wide I/O 3-D components, such as stacked DRAM cells [3].

Previous research shows that the crosstalk in a TSV array is a critical design issue due to the relatively large TSV dimensions and the increased number of aggressors compared to the traditional 2-D metal wires [4]. Crosstalk is a pattern dependent phenomena and a threat to the delay, the power consumption and the signal integrity [5].

Although, existing formulas to extract the parasitic elements in a TSV array [6, 7, 8, 9] enable simulating the pattern dependent TSV performance with circuit simulators, the need for a high-level crosstalk model is inevitable for two reasons. Firstly, for system simulators, implemented in high-level languages (e.g. SystemC) [10, 11, 12], which estimate the data stream dependent performance. Sec-

ondly, for the community working with the optimization of interconnect architectures through coding [13].

The dominant crosstalk source in a TSV array is the capacitive coupling [14]. Thus, the high-level crosstalk estimation, must be based on a simple, universally valid and scalable capacitance model. The previously used model [15, 16, 17, 18] assumes that the coupling capacitances between non-adjacent TSVs can be neglected because of the Faraday cage effect. This is accurate in the middle of an array, where the TSVs are enclosed by at least four adjacent TSVs (one in each cardinal direction), but not at the edges [19]. Additionally, the model claims that the coupling capacitances can be modeled using two different values: one for direct adjacent TSVs, and one for diagonal adjacent TSVs. This is not accurate, due to the TSV E-field sharing effect, discussed in [8, 20], which can influence the size of the coupling capacitances at the edges by up to 50 %. Moreover, structures adjacent to the TSV array (e.g. guard rings [21]) additionally influence the size of the edge coupling capacitances. Adjacent structures can cause a drastic increase of the self capacitances at the edges of a TSV array. At the edges, the self capacitances may even compete in strength with the coupling capacitances, while they are magnitudes smaller in the middle of the array due to the Faraday cage effect. The traditional model neglects all TSV self capacitances.

Summarized, for real TSV arrays, the previously used model is only valid for the TSVs located in the middle, and not at an edge of the TSV array. In contrast to the traditional 2-D metal-wires, where only two wires are located at the edges, in a $M \times N$ via array, $2M + 2N - 4$ vias

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are located at the edges. For example, in a 8×8 array (64b), 44% of the TSVs are edge TSVs. The edge effects are of paramount importance. In the case study presented in this work, we show that existing TSV coding techniques are impractical for real applications due to the edge effects.

The previous considerations show the need to extend the traditional TSV capacitance model, used for the estimation of the pattern dependent TSV performance, by the edge effects. This is the main contribution of this work. The presented model shows a low complexity, is scalable and yet provides a high accuracy. To derive the eight model parameters for one technology, the extraction of eight capacitance values for one exemplary array is sufficient. By means of these eight parameters, all capacitance values for all arbitrary TSV lengths and array dimensions can be predicted accurately. This ensures reusability and drastically reduces the time required for the full chip parasitic extraction, which is usually performed by means of cost intensive EM simulations. As an illustration, the actual total amount of capacitances in a single 8×8 (64b) array is already 2080, and they can be modeled with eight parameters.

2. Performance Metrics of TSV Arrays

In this section we outline why an accurate, an yet abstract TSV capacitance model is of tremendous importance for the design of TSV interconnect architectures. The two important performance metrics for interconnects are power consumption and delay, which are determined by the capacitive coupling. The heat dissipation, known as another important design metric for 3-D integration [1], is directly related to the power dissipation and consequently not listed as an independent performance metric.

In Ref. [15] we show that the dynamic energy extracted from the power supply, due to TSV_{*i*}, is equal to:

$$E_i = V_{dd}^2 b_i^+ \left(\sum_j C_{i,j} (\Delta b_i - \Delta b_j) + \Delta b_i (C_{G,i} + C_D) \right), \quad (1)$$

while the overall dissipated energy (transformed to heat) of the TSV array is equal to:

$$E_h = \frac{V_{dd}^2}{2} \left(\sum_{i,j} C_{i,j} (\Delta b_i - \Delta b_j)^2 + \sum_i \Delta b_i^2 (C_{G,i} + C_D) \right). \quad (2)$$

In Eq. 1-2, $C_{i,j}$ is the coupling capacitance between TSV_{*i*} and TSV_{*j*}, while $C_{G,i}$ is the overall ground capacitance connected to TSV *i*, which is composed of the TSV self capacitance $C_{i,0}$ and the connected load capacitance C_l . C_D is the effective capacitance of the driver. b_i^+ is the logical binary value on TSV *i* in the actual clock cycle and Δb_i is the difference between the binary value in the current (b_i^+) and the previous (b_i^-) clock cycle ($\Delta b_i = b_i^+ - b_i^-$).

The propagation delay T_i , of a capacitive interconnect structure can be estimated using [5]:

$$T_i = \Delta b_i^2 \left(0.69 R_E \left(\sum_j (1 - \Delta b_i \Delta b_j) C_{i,j} + C_{G,i} \right) + \kappa_D \right). \quad (3)$$

Here, R_E is the sum of the equivalent resistance of the driver R_D and the interconnect resistance R_I . For TSVs, R_I is usually significantly smaller than 1Ω [15]. Thus, $R_D \gg R_I$ and $R_E \approx R_D$. κ_D is an additive time constant due to the delay of the driver.

Eq. 1-3, combined with an abstract high-level capacitance model, are used to obtain high-level formulas for the pattern dependent TSV array performance [15, 16, 17, 18].

Although, existing formulas to extract the parasitic elements in a TSV array [6, 7, 8, 9] enable simulating the pattern dependent TSV energy consumption with circuit simulators, such high-level formulas are inevitable for two reasons.

Firstly, since delay and energy consumption are pattern dependent phenomenas, the most promising solution to improve the performance of an interconnect structure is modifying the transmitted data, using a coding process [13]. An abstract and yet accurate model, accessible at the high levels of abstraction, mapping the pattern properties to the energy consumption and delay, is required for the derivation and a fast evaluation of these coding schemes.

Secondly, the need for a high-level model is also inevitable for system simulators, typically implemented in high-level languages (e.g. SystemC) [10, 11, 12]. The interconnect architecture of a modern processor system has a throughput of several GB/s. This data rate makes it almost impossible to perform a simulation of the application specific energy requirements of such a system at the circuit level. For the simulation of the TSV energy consumption of a single modern 4×5 TSV array transmitting only 128 kB of data with a clock frequency of 1 GHz, we obtain a simulation time of ca. 38 ks for the circuit simulations on a modern Linux Xeon E5 machine with 512 GB of RAM. The simulation time increases quadratically with increasing TSV array dimensions, and linearly with an increasing pattern count. In contrast, a high-level simulation, based on a scalable capacitance model, only takes fractions of a second and the simulation time only slightly, linearly increases with an increased pattern or TSV count. For system simulations with data sets containing millions of patterns and dozens of TSVs, this means a speed up of more than 10^6 .

3. TSV Edge Effects

In this section, we first discuss the parasitic extraction of the TSV capacitances. Afterwards, in Section 3.2, a detailed discussion of the TSV edge effects is presented.

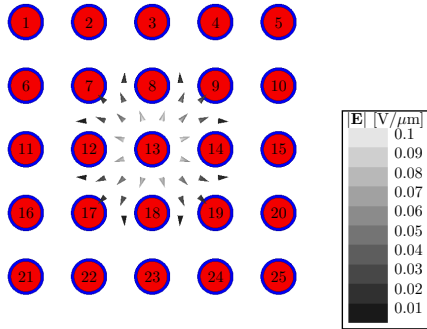


Figure 1: E-field vectors for a potential of 1 V on middle TSV₁₃

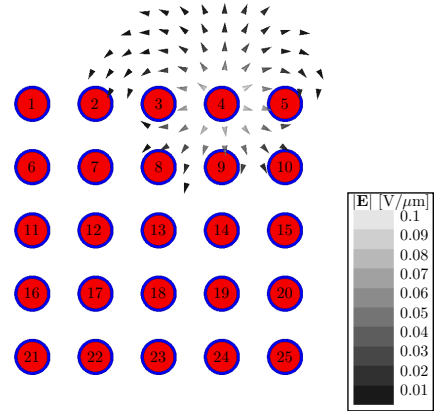


Figure 2: E-field vectors for a potential of 1 V on edge TSV₄

3.1. TSV Parasitic Extraction

Most previous work about TSV parasitic extraction is focused on arrangements of two TSVs. Thus, the already carried out research on TSV array edge effects is rather limited, even when addressing the lower levels of abstraction. In the reported literature, no work focuses on the influence of adjacent structures on the self and coupling capacitances of TSV arrays. The TSV E-field sharing effect and the effect of adjacent structures cannot be investigated individually, as they affect each other.

Consequently, in this work, the capacitance values are extracted by means of quasi-static parasitic extractions. For all later analyzed structures, the relative error of the electric field within the electro-quasi-static approximation, according to Ref. [22], is smaller than 0.1%. Therefore, the parasitic extraction in this work is performed by the quasi-static EM-wave solver Ansys Q3D Extractor. For this purpose, a 3-D structure of the TSV array is created.

The 2-D view of the structure is depicted in Fig. 1, which is used in Section 3.2 to illustrate the E-field distribution. The TSVs are regularly placed in the $M \times N$ array and indexed as TSV _{i} , where $m_i = \text{mod}(i, N)$ and $n_i = \text{ceil}(i/N)$ are the row and column location of TSV _{i} in the array, respectively. The distance between the centers of two direct neighbored vias is constant and denoted by d_{min} . Thus, the distance between any two diagonal neighbored vias is $\sqrt{2}d_{min}$. The cylindrical TSVs of length l_{tsv} and radius r_{tsv} are made up of copper. The TSVs traverse through the doped silicon substrate. The substrate conductivity σ is 10^5 S/m . For DC insulation, each TSV is surrounded by a SiO₂ dielectric of thickness $t_{ox} = r_{tsv}/5$. This value is chosen according to existing process nodes. In the model, the geometry parameters (d_{min} , l_{tsv} and r_{tsv}), and the significant frequency of the signals can be arbitrarily defined to model different process nodes. A TSV, its dielectric and the substrate form a metal oxide semiconductor (MOS) junction. Thus, in the substrate, a TSV is surrounded by a depletion region [23]. The width of the depletion region is calculated for every geometrical variation by means of the exact Poisson's equation for an

average TSV voltage of $\frac{V_{dd}}{2} = 0.5 \text{ V}$, and modeled as an area where the substrate has no free charge carriers ($\sigma=0$) [9].

3.2. TSV E-Field Distribution/Coupling

The field vectors are the source of the capacitances. Therefore, to outline the TSV edge effects on the capacitances, we analyze the electrical field vectors (\mathbf{E}) in TSV arrays, under different scenarios. For this analysis, the Ansys suite is used to draw the 2-D field vectors for different conductor potentials. For the sake of clarity, only vectors with an absolute value bigger than 5% of the maximum one are drawn.

First we analyze the field distribution of an exemplary 5×5 array with $r_{tsv} = 2 \mu\text{m}$ and $d_{min} = 8.5 \mu\text{m}$ surrounded by a $5 d_{min}$ Keep-out-Zone (KOZ). Hence, no component is placed in the substrate within a distance of $5 d_{min}$ from the array. After $5 d_{min}$, we assume the substrate to be grounded. In Fig. 1 the field distribution is illustrated for a potential of 1 V on middle TSV₁₃ while all remaining TSVs are grounded. As expected, in the middle of an array, only coupling in between adjacent TSVs has to be considered, since all adjacent TSVs form a Faraday cage which terminates E-field vectors. Consequently, the coupling between adjacent TSVs is mainly through the two sides of the TSVs which are facing each other. Since the absolute values of \mathbf{E} decrease with an increasing distance from TSV₁₃, the coupling between diagonal adjacent TSVs is lower than the coupling between direct adjacent TSVs.

Secondly, we analyze the edge effects. Every TSV not located at an edge of an array is enclosed by a Faraday cage, and consequently only couples with adjacent TSVs over their facing side. Therefore, the edge effects only significantly influence the coupling in between two TSVs which are both located at an edge of the array and only edge TSVs show a significant bulk/self capacitance. In Fig. 2 and Fig. 3 the E-field distributions for a potential of 1 V only on TSV₄ (located at one edge of the array) and only on TSV₅ (located at a corner/two edges) are illustrated, respectively. In this scenario, between edge TSVs the E-field increases significantly as none of the TSVs is enclosed

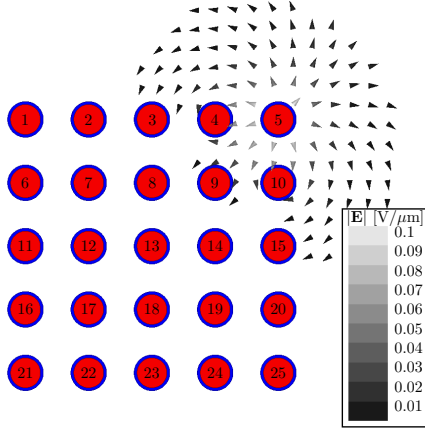


Figure 3: E-field vectors for a potential of 1 V on corner TSV₅

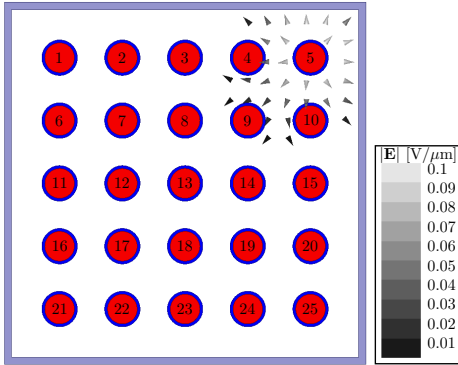


Figure 4: E-field vectors for a potential of 1 V on corner TSV₅ and a surrounding grounded metal ring

by a Faraday cage and the free substrate (KOZ) enables new paths for the field. Corner TSVs couple with other edge TSVs through three of the four sides since they are surrounded by only two horizontal/vertical adjacent TSV. The remaining edge TSVs couple with other edge TSVs through two sides since they are surrounded by three horizontal/vertical adjacent TSVs. Therefore, the coupling associated with a corner TSV is larger. At the edges, the coupling between horizontal or vertical indirect neighbored TSVs (e.g. TSV₃ and TSV₅) also increases significantly.

Finally, we discuss the effect of adjacent structures located nearby a TSV array. As an example, we analyze the E-field distribution in a TSV array which is surrounded by a grounded metal ring. In Fig. 4 the field distribution for a ring separation of $6.5\ \mu\text{m}$ and a voltage of 1 V on edge TSV₅ is illustrated. We only consider an edge TSV since, due to the Faraday cage effect, adjacent structures can only influence the E-field lines associated with edge TSVs. E-field lines terminate on a conductors surface. Since the metal ring is not isolated from the conductive substrate, the E-field lines are heavily drawn by the metal ring. This reduces the electric field lines in between the

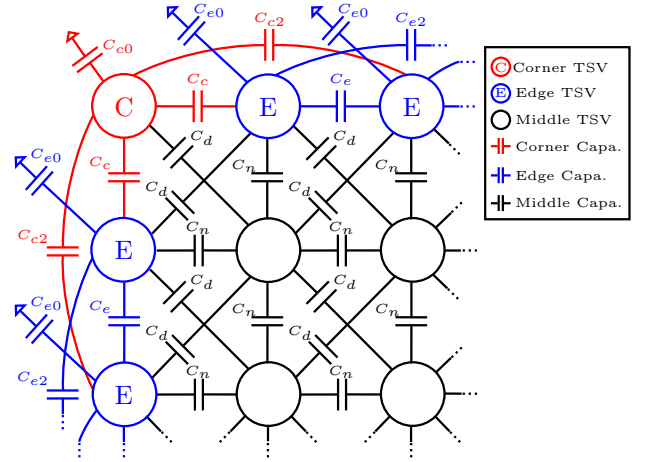


Figure 5: TSV capacitance model with edge effects

TSVs, which results in lower coupling capacitance values and drastically higher self capacitance values at the edges, especially at the corners.

4. TSV Capacitance Model

By considering the previously discussed TSV E-field distribution, we state the TSV capacitance model illustrated in Fig. 5. The coupling capacitance value between two edge TSVs generally differs from its counterpart in the middle of the array. Also, the TSV self capacitance values increase at the edges. If a TSV is not only located at one edge of the array but at a corner, this additionally influences the capacitance values connected to the TSV. Consequently, we distinguish between capacitances connected to at least one middle TSV (marked black in Fig. 5) and capacitances connected only to edge TSVs. For the second case, we also have to consider whether one TSV is located at a corner of the array (marked red in Fig. 5) or not (marked blue in Fig. 5).

The coupling capacitance value between any two direct adjacent TSVs, where at least one TSV is located in the middle of the array, is equal to C_n . In the following we will normalize the remaining capacitance values by C_n . This results in coefficients, independent of the TSV length. Additionally, the normalization helps to outline the critical capacitance values for crosstalk minimization. Even though a coupling capacitance between two edge TSVs over a corner (e.g. 5×5 array: between TSV₄ and TSV₁₀) is in some cases slightly bigger than the internal one, in the model we use a single parameter called C_d to define all capacitance values in between diagonal adjacent TSVs. The ratio between C_d and C_n is expressed by $\lambda_d = C_d/C_n$.

The capacitance value between a corner TSVs and its two direct adjacent edge TSVs is referred to as C_c ($\lambda_c = C_c/C_n$), while the capacitance value between a direct adjacent edge TSV pair, not located at a corner of the array, is referred to as C_e ($\lambda_e = C_e/C_n$). At the edges we consider the coupling between indirect (second order) adjacent edge TSVs. For the coupling capacitance between a corner TSV

Table 1: Model coefficients for TSV arrays surrounded by a KOZ

r_{tsv} [μm]	d_{min} [μm]	f [GHz]	$C_n(f)$ [$\text{fF}/20\mu\text{m}$]	$\lambda_d(f)$	$\lambda_{e0}(f)$	$\lambda_c(f)$	$\lambda_{e2}(f)$	$\lambda_{e0}(f)$	$\lambda_e(f)$	$\lambda_{e2}(f)$
1	4	11, 31	1.68, 1.47	0.31, 0.28	0.14, 0.17	1.40, 1.36	0.24, 0.21	0.06, 0.08	1.31, 1.28	0.18, 0.16
1	4.5	11, 31	1.53, 1.30	0.33, 0.30	0.18, 0.21	1.45, 1.42	0.25, 0.23	0.09, 0.10	1.34, 1.32	0.20, 0.18
2	5.5	11, 31	2.43, 2.26	0.22, 0.19	0.14, 0.14	1.39, 1.33	0.16, 0.13	0.07, 0.07	1.31, 1.27	0.11, 0.10
2	8	11, 31	1.86, 1.52	0.30, 0.28	0.23, 0.28	1.39, 1.37	0.20, 0.19	0.12, 0.14	1.31, 1.29	0.15, 0.15
2	8.5	11, 31	1.80, 1.45	0.30, 0.28	0.27, 0.32	1.39, 1.37	0.20, 0.20	0.13, 0.15	1.31, 1.29	0.15, 0.15
2.5	10	11, 31	1.89, 1.55	0.32, 0.30	0.26, 0.30	1.36, 1.34	0.19, 0.19	0.14, 0.16	1.29, 1.27	0.14, 0.14
4	12	11, 31	2.44, 2.09	0.25, 0.23	0.28, 0.29	1.37, 1.33	0.15, 0.14	0.12, 0.14	1.29, 1.26	0.11, 0.11
4	15	11, 31	2.03, 1.62	0.28, 0.26	0.18, 0.22	1.39, 1.37	0.18, 0.18	0.09, 0.11	1.30, 1.29	0.13, 0.14

Table 2: Model errors, normalized by C_n , for TSV arrays surrounded by a KOZ

r_{tsv} [μm]	d_{min} [μm]	l_{tsv} [μm]	f [GHz]	$M \times N$	Presented Model		Previous Model [15]	
					RMSE(f)	MAE(f)	RMSE(f)	MAE(f)
1	4	20	11, 31	5×5	0.018, 0.016	0.070, 0.062	0.175, 0.159	0.432, 0.387
1	4.5	20	11, 31	5×5	0.028, 0.026	0.093, 0.084	0.197, 0.183	0.485, 0.445
2	5.5	20	11, 31	5×5	0.006, 0.006	0.028, 0.027	0.164, 0.142	0.402, 0.340
2	8	20	11, 31	5×5	0.012, 0.014	0.056, 0.059	0.168, 0.168	0.393, 0.393
2	8.5	20	11, 31	5×5	0.015, 0.017	0.064, 0.069	0.169, 0.167	0.397, 0.475
2.5	10	20	11, 31	5×5	0.016, 0.016	0.033, 0.038	0.161, 0.156	0.372, 0.345
4	12	20	11, 31	5×5	0.008, 0.008	0.017, 0.019	0.156, 0.146	0.374, 0.334
4	15	20	11, 31	5×5	0.009, 0.011	0.037, 0.043	0.164, 0.160	0.390, 0.372
1	4	50	11, 31	7×7	0.019, 0.016	0.071, 0.064	0.155, 0.138	0.454, 0.398
1	4.5	50	11, 31	7×7	0.018, 0.018	0.078, 0.072	0.157, 0.143	0.455, 0.411
2	5.5	50	11, 31	7×7	0.006, 0.005	0.027, 0.023	0.134, 0.117	0.390, 0.338
2	8	50	11, 31	7×7	0.010, 0.026	0.052, 0.061	0.141, 0.133	0.415, 0.384
2	8.5	50	11, 31	7×7	0.020, 0.031	0.062, 0.074	0.141, 0.136	0.413, 0.393
2.5	10	50	11, 31	7×7	0.018, 0.018	0.033, 0.039	0.164, 0.158	0.380, 0.347
4	12	50	11, 31	7×7	0.008, 0.009	0.018, 0.019	0.159, 0.147	0.371, 0.337
4	15	50	11, 31	7×7	0.009, 0.010	0.040, 0.047	0.135, 0.131	0.390, 0.372

and its two indirect neighbored edge TSVs, we use the parameters C_{c2} and λ_{e2} . C_{c2} and λ_{e2} express the coupling capacitance between two indirect neighbored edge TSVs, both not located at a corner of the array.

The ground capacitance values are C_{c0} ($\lambda_{c0} = C_{c0}/C_n$) for the corner TSVs, and C_{e0} ($\lambda_{e0} = C_{e0}/C_n$) for the remaining edge TSVs. All other capacitances are set to zero.

Consequently, to determine all model coefficients, eight capacitance values, extracted for one exemplary TSV array, are required. By means of these capacitances, one can easily construct the capacitance matrix for arbitrary array dimensions $M \times N$ and TSV lengths.

5. Experimental Results

In this section, we determine the accuracy of the presented TSV capacitance model and compare it with the previously used model. Besides that, we report typical values for the model coefficients and analyze how they vary with the TSV array parameters. Additionally, we analyze the usability of the model for a fast estimation of the TSV performance metrics by means of Eq. 1.

For the TSV dimensions we choose several values based on the global TSV dimensions reported for the 2012-2018 time slot of the ITRS. For the extraction of the model coefficients, we assume a fixed TSV length of $20 \mu\text{m}$. Thus, for other TSV length the subsequently reported C_n values have to be scaled by $l_{tsv}/20 \mu\text{m}$. For all analyzed geometrical TSV array dimensions, the model coefficients are determined by means of quasi static extractions for a 5×5

array. The quasi static extractions are performed in the frequency range from 6 GHz to 31 GHz. In a TSV array, the maximum frequency that needs to be considered is given not by the clock, but by the rise and fall transition times. 6 GHz corresponds with a rise/fall time of ca. 0.1 ns, while 31 GHz corresponds with a rise/fall time of ca. 20 ps [24].

The remainder of this section is divided into four subsections. In Section 5.1 and Section 5.2 we analyze the accuracy of the capacitance model. A parametric analysis, to outline how the model coefficients change with the TSV array parameters, is presented in Section 5.3. Finally, in Section 5.4 the accuracy of the high-level energy estimation, based on the capacitance model, is investigated.

5.1. Model and Accuracy for TSV Arrays with a KOZ

For this analysis we assume that KOZs of $5 d_{min}$ surround the TSV arrays. For all analyzed geometrical TSV array dimensions and frequencies, the resulting model coefficients are listed in Table 1. The table reveals that the edge effects lead to a significant increase in the capacitance values. For example, the coupling capacitance value between direct adjacent TSVs at the corners is about 35%-40% bigger than the maximum coupling capacitance value in the middle of an array, as the reported λ_c coefficients are all in the range from 1.33 to 1.45. This validates the necessity to include the edge effects into the TSV capacitance model. For a KOZ around the array, the edge self capacitances are way smaller than the coupling capacitances, as the coefficients λ_{c0} and λ_{e0} do not exceed 0.32.

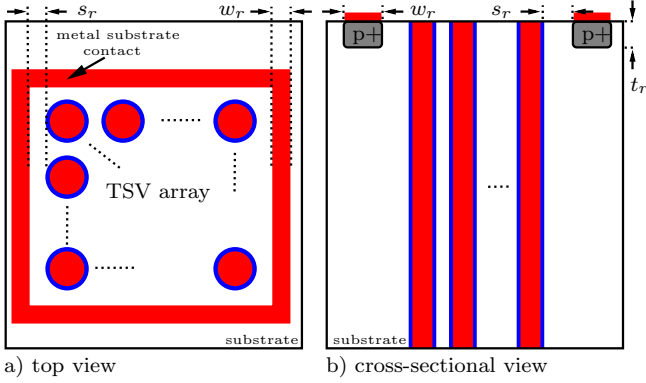


Figure 6: Structure of a p_+ ring for substrate noise suppression

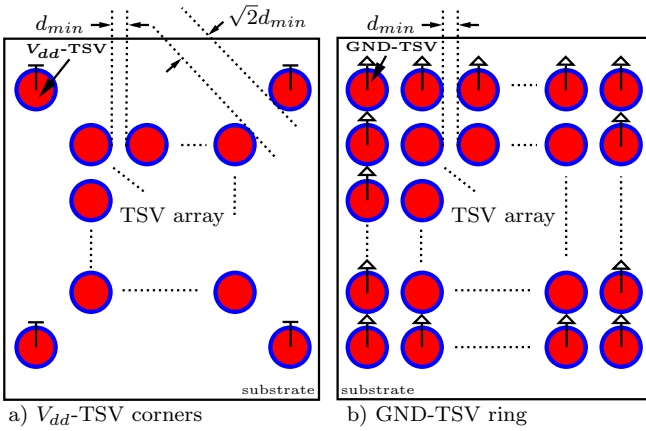


Figure 7: TSV array structures with adjacent V_{dd} /GND-TSVs

To analyze the model accuracy, the coefficients from Table 1 are used to reconstruct the capacitance matrix of the 5×5 arrays. Additionally, to show the reusability of the model, the coefficients (extracted for a 5×5 array and a TSV length of $20 \mu\text{m}$) are used to construct the capacitance matrix of 7×7 arrays with a TSV length of $50 \mu\text{m}$. All constructed matrices are compared with the capacitance matrices obtained by means of quasi static extractions of the respective array. The resulting root-mean-square-errors (RMSEs) and maximum-absolute-errors (MAEs) of the presented model, normalized by C_n , are illustrated in Table 2. For comparison purposes, the error values for the previous model are reported as well.

The table reveals that the errors of the presented model do not exceed $0.1 C_n$, while the previous model shows errors of up to $0.5 C_n$. According to the ITRS, the minimum radius and spacing of global TSV interconnects will decrease until 2019 to $1 \mu\text{m}$ and $4 \mu\text{m}$, respectively. For these geometrical parameters and a 5×5 array the presented model shows a RMSE reduction to almost a tenth and a MAE reduction to less than a sixth.

5.2. Model and Accuracy for TSV Arrays without a KOZ

Before we analyze the influence of adjacent components nearby the TSV array, we will shortly discuss which components are commonly placed nearby TSV arrays. Without a KOZ, the TSV substrate noise can drastically increase the failure rate of active components [21]. In fact, no active component can be placed directly adjacent to the TSVs due to their substrate noise. To reduce the substrate noise of a TSV array, p_+ guard rings are proposed [21]. The principle of a guard ring is to provide a low impedance path to the ground, so that a large part of the coupling noise is captured by the ring. Besides guard rings, a TSV array is often surrounded by power (V_{dd}) or ground (GND) TSVs. On the one hand, V_{dd} /GND-TSVs reduce the substrate noise; on the other hand they are required to generate a power/ground network that spans over the multiple dies of the 3-D SoC. As briefly discussed in Section 2.2, these structures also influence the edge effect coefficients, while the model parameters C_n and λ_d remain unchanged, compared to the arrays surrounded by a KOZ.

In this subsection, the model coefficients are analyzed for three exemplary noise reduction methods. Noise reduction method number one is a p_+ guard ring illustrated in Fig. 6. A p_+ ring is constructed by a p_+ well and a metal which is connected to the ground potential. We assume the thickness of the p_+ well, t_r , to be 5% or 15% of the substrate thickness ($l_{t_{sv}}$). The TSV array to ring spacing r_s is assumed to be equal to the minimum TSV spacing. The ring width w_r is $2 \mu\text{m}$. As illustrated in Fig. 7, in scenario two, the TSV array is surrounded by four V_{dd} -TSVs at the corners, and in scenario three by a ring of GND-TSVs. The resulting model coefficients for some TSV dimensions, which vary from the ones reported in Table 1, are listed in Table 3.

The table reveals that for all analyzed scenarios the self capacitance value of the corner TSVs exceeds C_n . In most of the cases, the self capacitance value is even the biggest capacitance value in the array. In general, at the edges, the self capacitances increase drastically. This again validates the necessity to include the edge effects in the TSV capacitance model. Additionally, as expected, the adjacent structures decrease the edge effects on the coupling capacitances. Even though, for most scenarios, the edge coupling capacitances are still significantly bigger than the ones in the middle, the coupling between indirect adjacent neighbors often decreases strongly. Therefore, in some scenarios, the coefficients λ_{c2} and λ_{e2} can be set to zero to reduce the model complexity.

The resulting models are again used to reconstruct the capacitance matrices of the TSV arrays. The resulting RMSE and MAE values, normalized by C_n , are presented in Table 4. For comparison purposes, the values for the previously used model are listed as well. For all matrices, the RMSE values do not exceed 2.3% of C_n with our approach, while the RMSE of the previous approach shows

Table 3: Varying model coefficients for the TSV arrays with varying adjacent structures

Adjacent Structure	r_{tsv} [μm]	d_{min} [μm]	f [GHz]	$\lambda_{c0}(f)$	$\lambda_c(f)$	$\lambda_{c2}(f)$	$\lambda_{e0}(f)$	$\lambda_e(f)$	$\lambda_{e2}(f)$
p_+ ring ($t_r=0.05l_{tsv}$)	1	4	11, 31	1.11, 1.09	1.27, 1.24	0.17, 0.14	0.58, 0.55	1.22, 1.20	0.13, 0.11
p_+ ring ($t_r=0.15l_{tsv}$)	1	4	11, 31	1.53, 1.47	1.21, 1.18	0.14, 0.12	0.80, 0.80	1.17, 1.16	0.12, 0.10
V_{dd} -TSV corners	1	4	11, 31	1.35, 1.27	1.25, 1.23	0.16, 0.14	0.46, 0.45	1.28, 1.25	0.16, 0.14
GND-TSV ring	1	4	11, 31	3.03, 2.92	0.97, 0.98	0.02, 0.02	1.69, 1.65	0.99, 0.99	0.03, 0.03
p_+ ring ($t_r=0.05l_{tsv}$)	2	8.5	11, 31	1.13, 1.02	1.26, 1.22	0.10, 0.08	0.56, 0.53	1.22, 1.18	0.08, 0.06
p_+ ring ($t_r=0.15l_{tsv}$)	2	8.5	11, 31	1.58, 1.42	1.20, 1.17	0.08, 0.06	0.82, 0.76	1.17, 1.14	0.06, 0.05
V_{dd} -TSV corners	2	5.5	11, 31	1.24, 1.11	1.27, 1.24	0.09, 0.08	0.37, 0.34	1.29, 1.25	0.10, 0.08
GND-TSV ring	2	5.5	11, 31	2.70, 2.59	1.01, 1.00	0.00, 0.00	1.45, 1.39	1.01, 1.00	0.00, 0.00

 Table 4: Model errors, normalized by C_n , for the TSV arrays with varying adjacent structures

Adjacent Structure	r_{tsv} [μm]	d_{min} [μm]	l_{tsv} [μm]	f [GHz]	Presented Model		Previous Model [15]	
					RMSE(f)	MAE(f)	RMSE(f)	MAE(f)
p_+ ring ($t_r=0.05l_{tsv}$)	1	4	20	11, 31	0.014, 0.012	0.045, 0.034	0.293, 0.291	1.122, 1.102
p_+ ring ($t_r=0.15l_{tsv}$)	1	4	20	11, 31	0.013, 0.012	0.035, 0.036	0.398, 0.389	1.535, 1.474
V_{dd} -TSV corners	1	4	20	11, 31	0.023, 0.022	0.114, 0.103	0.304, 0.287	1.368, 1.280
GND-TSV ring	1	4	20	11, 31	0.014, 0.015	0.052, 0.058	0.836, 0.806	3.084, 2.964
p_+ ring ($t_r=0.05l_{tsv}$)	2	8.5	20	11, 31	0.005, 0.005	0.019, 0.018	0.311, 0.285	1.131, 1.029
p_+ ring ($t_r=0.15l_{tsv}$)	2	8.5	20	11, 31	0.005, 0.004	0.021, 0.018	0.427, 0.388	1.589, 1.427
V_{dd} -TSV corners	2	5.5	20	11, 31	0.017, 0.014	0.085, 0.069	0.290, 0.257	1.246, 1.104
GND-TSV ring	2	5.5	20	11, 31	0.005, 0.004	0.017, 0.013	0.731, 0.877	2.706, 2.592

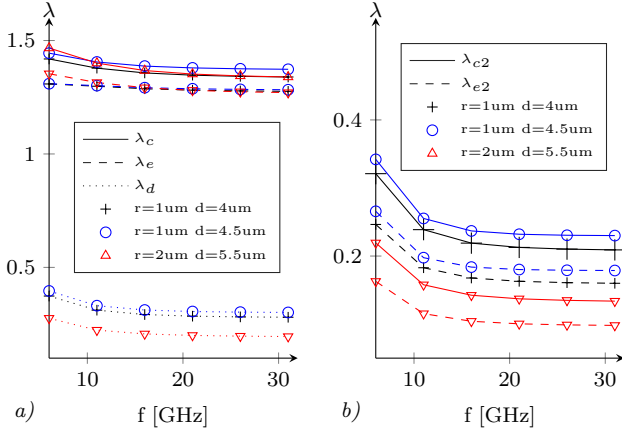


Figure 8: Model coefficients for three different TSV arrays over the frequency: a) capacitive coupling between direct neighbored TSV; b) capacitive coupling between indirect neighbored TSV

values of up to 83.6% of C_n . Due to the discussed corner self capacitances, the previously used capacitance model always shows errors bigger than C_n (maximum ca. $3.1C_n$). In comparison, the maximum error of the presented model is again about $0.1C_n$.

Summarized, the experimental results show that the proposed TSV capacitance model shows a way higher accuracy than the previously used model. For all TSV capacitance matrices (with and without a KOZ) the presented model shows an normalized RMSE (NRMSE) of about 1.5% of C_n while the previous model shows an NRSME of 36.9%. This is a reduction by about 96%.

5.3. Parametric Analyses

For the parametric analyses, we vary various parameters of a 5×5 TSV array and analyze how these variations influence the model coefficients.

Firstly, we analyze the dependency of the model coefficients on the signal frequencies and the TSV dimensions. Therefore, for eight different TSV dimensions, and a surrounding $5d_{min}$ KOZ, we extract the model coefficients for various frequencies. The results, considering the capacitive coupling in three exemplary arrays, are illustrated in Fig. 8. The analysis shows that λ_c and λ_e are only slightly dependent on the TSV dimensions (r_{tsv} and d_{min}). The highest deviation occurs at a frequency of 6 GHz, where we get λ_c and λ_e values in the range from 1.40 to 1.47 and 1.30 to 1.36, respectively. In contrast, the remaining coefficients show a significantly higher dependency on the TSV dimensions. With increasing TSV radii and decreasing pitches, these coefficients and consequently the edge effects, decrease.

In the following, we will discuss the frequency dependency of the coefficients in detail. Since the substrate is conductive, its electrical behavior can be modeled as CG -parallel components in between the TSVs [9]. Therefore, the admittance of a substrate unit element is:

$$Y'_{subs} = j\omega C'_{subs} + G'_{subs}. \quad (4)$$

We introduce the lossy (complex) equivalent capacitance:

$$C'_{eq,subs} = \frac{Y'_{subs}}{j\omega} = C'_{subs} + \frac{G'_{subs}}{j\omega}. \quad (5)$$

The absolute value of $C'_{eq,subs}$ decreases with a $1/f$ like behavior and asymptotically reaches C'_{subs} . A decreasing $C'_{eq,subs}$ value leads to decreasing edge effects, since edge effects occur as extra substrate paths for the E-field. Consequently, the edge effects generally show an $\alpha + \frac{\beta}{f}$ behavior. With increasing substrate doping concentrations, and therefore increasing G'_{subs} values, the β values increase while the α values remain constant. Thus, with lower frequencies and higher doping concentrations, the edge effects increase. But, for very high frequencies, the edge effects

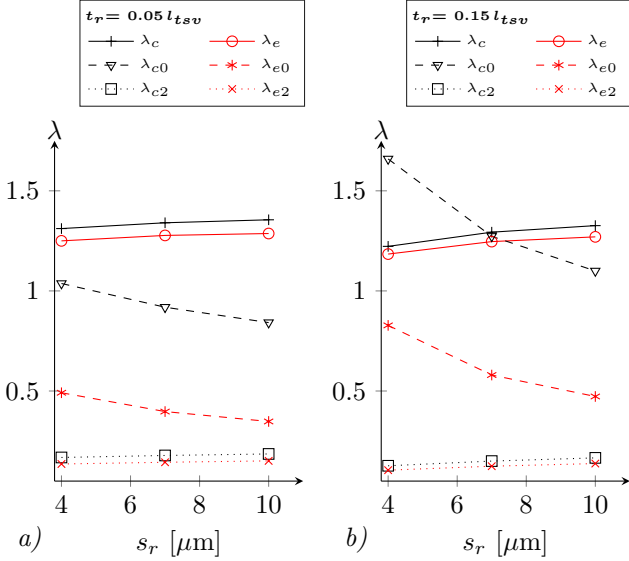


Figure 9: Model coefficients over the p_+ ring separation s_r for two diffusion depths t_r : a) $t_r=0.05 l_{tsv}$; b) $t_r=0.15 l_{tsv}$

are independent of the doping profile and equal to the α values. For all analyzed TSV arrays we measured α values of at least 1.31. Therefore, even for ultra high frequency applications and/or low doping profiles, the edge effects are still important.

As a second parametric analysis, we investigate the influence of the dimensions of a p_+ ring around a TSV array. In Fig. 9 the results for a 5×5 array ($r_{tsv}=1 \mu\text{m}$; $d_{min}=4 \mu\text{m}$; $f=11 \text{ GHz}$) with a fixed ring width w_r of $1 \mu\text{m}$ are illustrated. Here, we do not illustrate the influence of varying w_r , because it has a negligible effect: doubling w_r leads to a variation of the model coefficients of always less than 5%. The closer and the thicker the ring is, the more E-field lines it draws. Consequently, with a decreasing s_r and/or an increasing t_r , the coefficients related to the inter TSV coupling (λ_c , λ_e , λ_{c2} and λ_{e2}) decrease, while the coefficients related with the self capacitances (λ_{c0} and λ_{e0}) increase. Thus, a deep p_+ guard ring, located nearby the TSV array, can reduce the substrate noise and the inter TSV noise very effectively.

For the last analysis, we compare V_{dd} - and GND-TSVs with p_+ rings in terms of coupling noise reduction. Therefore, the model coefficients λ_c and λ_e in a 5×5 array ($r_{tsv}=1 \mu\text{m}$; $d_{min}=4 \mu\text{m}$) are analyzed. For various frequencies, the coefficients are extracted once for a $5d_{min}$ KOZ, once for V_{dd} /GND-TSV corners, once for V_{dd} /GND-TSV rings, and once for the p_+ rings from Section 4.2. The results are shown in Fig. 10. The figure reveals that a GND-TSV ring is the best method to reduce the inter TSV noise, as it yields to the smallest λ_c and λ_e coefficients. In general GND-TSVs slightly outperform V_{dd} -TSVs for low frequencies. This behavior occurs due to the MOS effect. With an increasing average TSV voltage, the width of its surrounding depletion region increases. A depletion region is a region where the usual conductive substrate

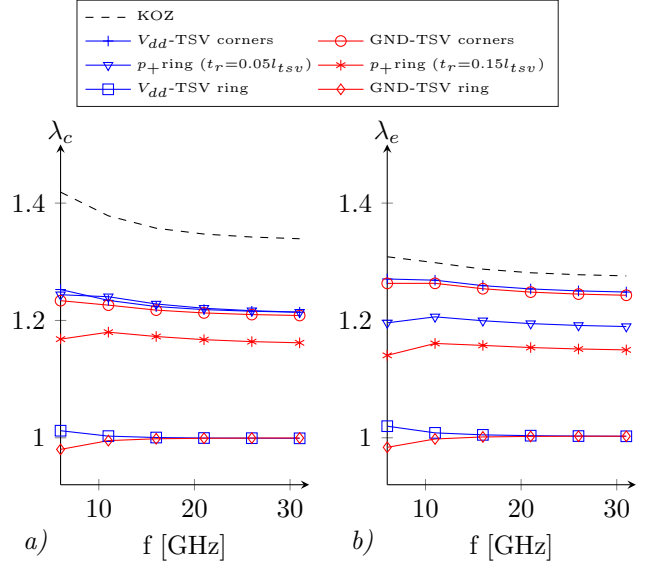


Figure 10: Comparison of the inter TSV coupling: a) λ_c ; b) λ_e for different adjacent V_{dd} /GND-TSV constellations and p_+ guard rings

has no free charge carriers ($\sigma=0$). Consequently, an increasing average TSV voltage increases its isolation from the substrate [9]. Thus, a V_{dd} -TSV draws generally less E-field lines than a GND-TSV. However, Eq. 4 shows that for $j\omega C'_{subs} \gg G'_{subs}$ the substrate conductance, and consequently the influence of a depletion region, can be neglected. Therefore, for very high frequencies, GND- and V_{dd} -TSVs can be seen as equivalent shielding structures. Additionally, both structures lead to a sufficient decrease of the substrate noise, due to the Faraday cage effect.

Even though p_+ rings cannot compete with a V_{dd} - or GND-TSV ring, they still show a significant reduction of the inter TSV coupling noise. Additionally, the area and production cost for a guard ring are lower than for TSV rings.

V_{dd} - or GND-TSV corners are able to reduce the coupling between corner and edge TSV by approximately 15%-20%. However, due to their location, their efficiency to reduce the coupling in between an edge TSV pair, not located at a corner, is very limited.

Summarized, one can state that a ring of stable TSVs leads to the biggest suppression of the coupling and substrate noise but also to a very big overhead. A trade-off between noise reduction and complexity offer p_+ rings. The least noise reduction, especially for large TSV arrays, occurs for stable corner TSVs. However, if either way some additional V_{dd} /GND-TSVs are required to setup the power/ground network over the multiple dies of the 3-D SoC, the overhead of four stable TSV corners as the shielding structure can be regarded as nearly zero.

5.4. Accuracy for the TSV Energy Estimation

After we have shown the accuracy of the presented capacitance model, in this subsection, we investigate the us-

Table 5: Maximum absolute error (MAE) and root means square error (RMSE) of the energy estimation, based on the presented and the previous TSV capacitance model, for all input pattern combinations in the 3×3 subarray. The values are normalized by the maximum (\bar{E}_{ex}) and mean (\hat{E}_{ex}) extracted energy of a TSV per clock cycle.

TSVs	Circuit+EM Simulations		Presented Model		Previous Model [15]	
	\bar{E}_{ex} [fJ]	\hat{E}_{ex} [fJ]	MAE [%]	RMSE [%]	MAE [%]	RMSE [%]
All	5.99	47.77	5.09	4.50	34.19	41.62
Edge	5.75	43.97	5.09	6.40	34.19	59.49
Middle	6.30	47.77	2.28	2.95	2.28	2.95

ability of the model for the estimation of the TSV performance metrics. For this purpose, we measured the energy consumption of the TSVs in a 3×3 subarray, in the corner of a 4×5 array, for all possible input pattern combinations, by means of Spectre circuit simulations. For the remaining TSVs in the array, the input switching is assumed to be random. We choose this specific experimental setup to investigate the influence of third order neighbors and the influence of non-quadratic array dimensions. To ensure an accurate simulation of the TSV array performance on the circuit level, the complete $3-\pi$ RLC circuit of the TSV array is extracted with the Q3D Extractor for: $r_{tsv}=1 \mu\text{m}$, $d_{min}=4 \mu\text{m}$, $l_{tsv}=50 \mu\text{m}$ and a $5 d_{min}$ KOZ. In the simulation, each TSV is driven by a two inverter chain and the input slew rate is 10 ps. The load of each TSV is equal to 1 fF. Driver strengths of the first and second inverter are $4 \times$ and $12 \times$, respectively. For the inverters 22 nm Predictive Technology Model (PTM) is used. For the drivers, we measured an average output rise time of ca. 50 ps. The $2^{18}=262,144$ patterns are transmitted with a pattern duration of 1 ns. The $9 \cdot 2^{18}=2,359,296$ energy quantities are measured by integrating the current flowing in the drivers multiplied by $V_{dd}=1 \text{V}$ in MATLAB. Thus, leakage is included in the results. The simulation time of the experiment is about 11 hours on a modern Intel Xeon E5 machine with 512 GB of RAM.

Additionally, the energy quantities are estimated using MATLAB and Eq. 1, in combination with the presented and the previously used capacitance model, which only takes fractions of a second. For the applied drivers, the effective capacitance C_D is about 1.7 fF.

The results are presented in Table 5. The results show that the neglected edge effects lead to a tremendous underestimation of the energy consumption of the edge TSVs, as the NRMSE almost reaches 60%. In comparison, the presented model, which takes the edge effect in an abstract way into account, only shows an NRMSE of 6.4% for the estimation of the edge TSV energy consumption. This represents an accuracy improvement by a factor of 9.3. The results also show that the edge effects have a significant impact on the overall energy consumption. Even though the previous and the presented model show the same low NRMSE (2.95%), for the estimation of the energy consumption of the middle TSVs, the overall NRMSE for the

traditional model is above 40%, while for the presented model it is below 5%. In terms of maximum error, the presented model leads to an improvement by a factor of 6.72, compared to the previously used model.

Summarized, the capacitance model, presented in this work, is the first capacitance model which enables an accurate estimation of the performance metrics of edge TSVs on a high level of abstraction.

6. Case Study

By means of this case study, we outline the tremendous importance of the edge effect for TSV coding techniques. Existing TSV coding schemes are solely designed to reduce the TSV crosstalk, which reduces the maximum TSV delay and the peaks in the power consumption. For the derivation of previous TSV coding approaches, the edge effects are not considered and the efficiency of the coding approach is only evaluated for the delay reduction of a TSV in the middle of an array where edge effects do not occur.

Existing TSV coding techniques, have in common, that for each TSV they reduce the maximum amount of direct adjacent TSVs switchings in the opposite direction, as these transitions cause the maximum delay increment and energy/power consumption (see Eq. 1-3 with $\Delta b_i=1$ and $\Delta b_j=-1$). For example, the $6C$ coding [16], simply limits the maximum amount of direct (horizontal/vertical) adjacent TSVs switching in the opposite direction to three. When three direct adjacent TSVs switch in the opposite direction, the remaining one always switches in the same direction. Consequently, for a middle TSV, the maximum energy consumption in a clock cycle is reduced from

$$V_{dd}^2((8 + 8\lambda_d)C_n + C_{i0} + C_D), \quad (6)$$

to

$$V_{dd}^2((6 + \lambda_d)C_n + C_{i0} + C_D), \quad (7)$$

while the maximum delay is reduced from

$$0.69R_E((8 + 8\lambda_d)C_n + C_{i0}) + \kappa_D, \quad (8)$$

to

$$0.69R_E((6 + \lambda_d)C_n + C_{i0}) + \kappa_D. \quad (9)$$

Edge TSVs have maximum three horizontal/vertical adjacent neighbors. Thus, for edge TSVs, the $6C$ coding does not affect the maximum amount of direct adjacent TSVs switching in the opposite direction. Coded and uncoded, the maximum energy consumption and delay are:

$$V_{dd}^2((2 + 2\lambda_c + 2\lambda_e + 4\lambda_d + 2\lambda_{e2} + \lambda_{e0})C_n + C_{i0} + C_D), \quad (10)$$

and

$$0.69R_E((2 + 2\lambda_c + 2\lambda_e + 4\lambda_d + 2\lambda_{e2} + \lambda_{e0}) + \kappa_D). \quad (11)$$

Since $2\lambda_c + 2\lambda_e + 2\lambda_{e2} + \lambda_{e0} > 4 + 4\lambda_d$, for all analyzed TSV arrays, due to the edge effects, the worst case delay/energy

Table 6: Performance metrics for a TSV interconnect architecture, transmitting a 16bit wide data stream, for existing coding schemes. Reported are the maximum delay for middle TSVs ($T_{max,m}$), edge TSVs ($T_{max,e}$) and all TSVs ($T_{max,a}$), as well as the power consumption for middle TSVs (P_m), edge TSVs (P_e) and all TSVs (P_a), according to circuit simulations in combination with EM field solver and according to the high-level models. Additionally, the gate equivalents (GE) of the CODECS and the number of required TSVs (NT) are reported

Data Stream	Circuit+EM Simulations						Presented Model						Previous Model						Others	
	P [μ W]			T_{max} [ps]			P [μ W]			T_{max} [ps]			P [μ W]			T_{max} [ps]			NT	GE
	m	e	a	m	e	a	m	e	a	m	e	a	m	e	a	m	e	a		
Unco.	25	70	95	120	110	120	25	69	94	121	108	121	25	50	75	121	85	121	16	0
6C	33	71	104	99	109	109	33	71	104	101	108	108	33	55	88	101	86	101	20	181
4LAT	39	103	142	94	104	104	40	105	147	96	101	101	40	83	123	96	78	96	27	1916
6C-FNS	28	92	120	79	112	112	28	91	119	78	111	111	28	79	98	78	86	86	24	718

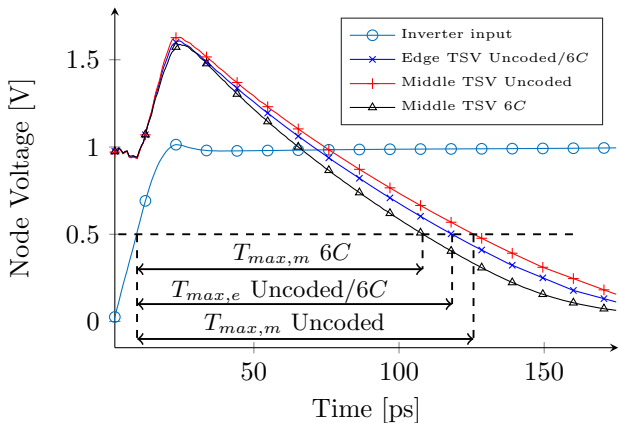


Figure 11: Worst case delay: inverter input and TSV output signals

consumption for the coded patterns occurs at the edges. Therefore, the edge effects reduce the coding efficiency.

In this case study, we analyze the coder/decoder circuit (CODEC), the number of required TSVs (NT), the maximum propagation delay (T_{max}), and the mean power consumption ($P = \frac{E}{NT_{clk}}$) for existing TSV coding approaches [16, 17, 18], as these are the design metrics of an interconnect architecture. We consider the transmission of a 16 bit wide random data stream, consisting of 10,000 patterns, over arrays of TSVs. To obtain the minimum number of TSVs for the 6C[16], 4LAT[17], and 6C-FNS[18] coding: a 5×4 , a 3×9 , and a 3×8 TSV array is required, respectively. In general, the 4LAT and the 6C-FNS coding always lead to a $3 \times x$ TSV array, which drastically increases the number of edge TSVs. In the analysis, the TSV dimensions are equal to the minimum ones reported for the year 2018 by the ITRS ($r_{tsv}=1 \mu\text{m}$; $d_{tsv}=4 \mu\text{m}$ and $l_{tsv}=50 \mu\text{m}$) and the arrays are surrounded by a $5 d_{min}$ KOZ. As in Section 5.4, reference values for the performance metrics are determined for the 22nm PTM technology by means of Spectre circuit simulations in combination with extracted RLC circuits. These reference values are compared with the estimations provided by the presented and the previous capacitance model, combined with Eq. 2 and Eq. 3.

In Fig. 11, the Spectre simulations for the maximum delay measurement are illustrated for the 6C coding. In this work, we distinguish between the maximum delay of a middle TSV ($T_{max,m}$) and the maximum delay of an edge

Table 7: Influence of existing coding schemes on the power consumption ($P' = P_{coded}/P_{uncoded}$) and the maximum propagation delay ($T' = T_{max,coded}/T_{max,uncoded}$). Reported are the values according to circuit simulations in combinations with field solvers and the estimations with the high-level models

Coding	EM+Circuit Simulations		Presented Model		Previous Model	
	P'	T'	P'	T'	P'	T'
6C	1.09	0.89	1.10	0.89	1.12	0.82
4LAT	1.50	0.85	1.54	0.83	1.56	0.78
6C-FNS	1.27	0.92	1.28	0.89	1.24	0.69

TSV ($T_{max,e}$), for the coded and the uncoded patterns. To determine the CODEC complexity, all encoder/decoder pairs are synthesized in a commercial 40 nm technology, and the resulting gate equivalents are reported.

The results are shown in Table 6. The results show that the worst case delay always occurs at the edges for the coded data streams. For the uncoded scenario, the highest delay occurs in the middle of the array, due to the bigger amount of aggressors. Due to the high fraction of edge TSVs, for reasonable array dimensions, the edge TSVs (e) have a several times higher power/energy consumption than the middle TSVs (m). Consequently, in the analyzed arrays 68%-85% of the overall TSV power consumption is caused by the edge TSVs. This underlines the importance of the edge effects.

This behavior is captured by the presented capacitance model. The presented model shows a very high accuracy: for the power consumption and the maximum delay estimations, the error values do not exceed 1.84% and 3.82%, respectively. In contrast, according to the previously used model, neglecting the edge effects, the worst case delay always occurs for the middle TSVs and a significantly lower fraction of the power consumption is caused by the edge TSVs. This generally leads to a dramatic overestimation of the performance metrics.

In Table 7, the resulting real delay reductions for the coding schemes are shown with the estimated values. The reported values for the delay reduction according to the previous model, correspond with the values reported in [16], [17] and [18], as they present the delay reduction of a middle TSV. However, since existing coding schemes were derived by means of the previous model, the authors could not identify the necessity to look at the edge TSVs for the evaluation of the delay reduction. The results show that

the edge effects drastically decrease the real delay reduction and consequently the efficiency of the coding schemes. For example, the delay reduction of the previously most promising coding approach (Ref. [18]) is only about 25% of the previously reported value. The other two coding schemes also show a degradation in the the delay reduction by over 30%, due to the edge effects. Additionally, all coding approaches lead to an increase in the overall TSV power consumption, which can be even bigger than 50%.

Summarized, the low gain in terms of delay reduction, caused by the edge effects, in combination with the high TSV area and power overhead, makes existing TSV coding schemes unsuitable for most applications. Therefore, circuit designers have to rethink the approach of constructing coding approaches by considering the edge effects. The fundamental for this new approach is the capacitance model, combined with high-level formulas, presented in this work, as the estimated performance metrics correspond well with the values for a 3-D EM-field solver in combination with circuit simulations.

7. Conclusion

In this paper we studied the impact of the edge effects on the TSV array performance. We proposed a simple, universal and scalable model to construct the capacitance matrices for arbitrary TSV array dimensions and TSV lengths by means of eight (simple extractable) model coefficients. This model extends the traditional model by six edge effect coefficients, which are adapted to the surrounding of the TSVs. Therefore, the model works for the typical KOZ around a TSV array, as well as for adjacent structures as V_{dd}/GND -TSVs or guard rings. This ensures a high model reusability. The model shows to be highly accurate compared with a 3-D field solver for 24 different modern TSV array structures (NRMSE: 1.5%), while the previously used model shows a $20\times$ higher NRMSE value (36.9%). This underlines the importance of considering the edge effects in the capacitance model. The main application of this capacitance model is the high-level estimation of the pattern dependent performance metrics of an interconnect structure. Experimental results reveal that the presented model, combined with simple high-level formulas, is highly accurate for the estimation of the TSV performance metrics on high levels of abstraction. Compared to the previously applied capacitance model, the RMSE can be reduced to almost one tenth.

In this paper, we additionally performed a case study which shows that existing CACs, derived by means of the previous model, are impractical due to the edge effects. For the CAC patterns, the edge effects lead to a significantly higher crosstalk for the edge TSVs, compared to the middle TSVs. In the case study we measured a decrease in the coding efficiencies due to the edge effects of up to 75%. Therefore, for the derivation of future coding approaches, the presented capacitance model needs to be considered.

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