Accounting for Current Degradation Effects in the Compact Noise Modeling of Nano-scale MOSFETs

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***Abstract*—This work presents a compact modeling approach and Verilog-A implementation method for flicker noise in MOSFETs, accounting for current degradation effects such as field-dependent mobility attenuation and access resistance. After arguing on the importance of such effects for noise level assessment, a Lambert-W based drain current model is utilized as an example to showcase the degradation-aware compact noise modeling. For the access resistance effects, measurements from nano-scale MOSFETs are utilized for experimental demonstration. Moreover, adapted methods for proper calculation of transconductance (intrinsic and extrinsic) as well as noise source positioning are also presented, revealing their significance for the correct model implementation.**

Keywords—Low-frequency noise; Mobility degradation; Access resistance; Verilog-A; Compact modeling; CMOS circuits

I. Introduction

The successful industrial-level production of nano-scale area MOSFETs has paved the way for the design and fabrication of circuits with unprecedented performance and capabilities in both analog and digital [1] systems. Some undesirable effects however, mainly related to the shrinking of the device channel length or the introduction of new materials and architectures, can limit the figures of merit and the design margins. Apart from the channel length modulation, the Drain-Induced Barrier Lowering (DIBL) and the threshold voltage roll-off [2] in nano-meter lengths, there is a more significant ON current degradation. The latter takes place, on one hand, due to the field-dependent mobility (intrinsic) degradation related to carrier scattering effects [3] and, on the other hand, due to the relative importance of the access resistance (extrinsic) at the source (S) and drain (D) regions, compared to the very low resistance of short channels.

On top of the non-ideal static (I-V) behavior, the area miniaturization, along with the implementation of non-planar architectures with alternative materials, results in an increase of low-frequency noise (LFN) levels [4]. The LFN is a critical technology figure of merit, as it relates directly to signal-to-noise degradation in amplifiers and sensors [5], as well as phase noise in oscillators and read/write errors in memories, when considering a time-domain particularity of LFN, called Random Telegraph Noise (RTN) [6]. Therefore the compact modeling of LFN/RTN effects to achieve precise CMOS circuit noise simulations is a requirement for the successful technological advancement through reliable circuit design. And it is equally critical to explore and properly model how the aforementioned current degradation effects in nano-scale devices can influence the noise behavior.

In one of the authors' recent works [7] it was experimentally demonstrated that the source-drain access resistance, R_{sd}, can lead to an apparent LFN level decrease and to an incorrect extraction of LFN-related parameters. The LFN model was adapted in [8], in order to provide an access resistance immune noise parameter extraction from experimental data. In this work, the implementation of this new modeling approach in Verilog-A is investigated. Before showing the possible difficulties one can encounter in terms of module connectivity and critical derivative calculations, an experimental demonstration of the access resistance effect on LFN is provided.

II. Impact of Degradation Effects on LFN

A. MOSFET LFN sources and modeling

The 1/f-like power spectral density, also called LFN, is a very common observation in MOSFETs. There are two competing approaches that aim to explain this type of noise: the "Carrier number fluctuations" (CNF) one [9], considering the LFN as a result of carrier trapping/de-trapping in interface traps, and the "Mobility fluctuations" approach [10], which attributes LFN to scattering effects occurring within the MOSFET channel. However, a combining approach has also been developed, considering that the CNF can also lead to "Correlated mobility fluctuations" (CMF) through carrier scattering near the fluctuating trapped charge [11]. The latter modeling method is expressed through (1) [12]:

$$S_{id} = g_m^2 S_{V_{fb}} \left(1 + \Omega \frac{I_d}{g_m}\right)^2 \tag{1}$$

where S_{id} is power spectral density of the drain current, I_d , $g_m=dI_d/dV_g$ the gate transconductance. S_{Vfb} is the flat-band voltage fluctuations power spectral density, and Ω is the CMF coefficient given by (2).

$$S_{V_{fb}} = \frac{q^2 \lambda k T N_t}{WLC_{ox}^2 f} \ , \ \Omega = \alpha_{sc} \mu_{eff} C_{ox} \tag{2}$$

where μ_{eff} is the effective mobility, C_{ox} the oxide capacitance per unit area, λ the dielectric tunneling constant (≈ 0.1 nm), kT is the thermal voltage, q is the electron elementary charge, f the frequency. N_t is the volumetric trap density ($/cm^3eV$), W, L are respectively the channel width and length, and α_{sc} is the remote Coulomb scattering coefficient. Based on the fact that the CNF/CMF model (1) has been globally proven valid for various CMOS technologies such as Bulk [12], FD-SOI, and FinFETs [13], the authors have chosen it to explore the current degradation effects and Verilog-A module implementation in this work.

As one can notice in (1), the noise level, S_{id}, is directly proportional to the square of the transistor's g_m, whereas the last part including the CMF factor Ω is proportional to I_d/g_m. Furthermore, it can be easily derived that the input-referred gate voltage noise (3), defined as $S_{Vg}=S_{id}/g_m^2$, would only contain the I_d/g_m term regarding the static parameters. The S_{Vfb} parameter is generally considered bias-independent.

$$S_{Vg} = S_{Vfb} \left(1 + \Omega \frac{I_d}{g_m}\right)^2 \tag{3}$$

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Since both the output (1) and input (2) LFN models contain the static-related terms I_d and g_m, it is worth exploring the degree in which a possible degradation of the device static behavior can affect the LFN and how it can be accounted for in the model.

B. Mobility attenuation effects

One main source of current degradation in MOSFETs stems from the electric field dependent attenuation of carrier mobility in the channel. This effect can be generally described through the effective mobility, μ_{eff}, expression (4), which includes both Coulomb (θ_1) and surface roughness (θ_2) scattering factors and the inversion charge density, Q_i.

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1\left(\frac{Q_i}{C_{ox}}\right) + \theta_2\left(\frac{Q_i}{C_{ox}}\right)^2} \quad (4)$$

In [14], Boutchacha and Ghibaudo showed that the mobility attenuation factors can be accounted for in (3), if I_d/g_m is replaced by (5), where V_t is the transistor's threshold voltage.

$$\mu_{eff}\frac{I_d}{g_m} = \mu_0\frac{V_g - V_t}{1 - \theta_2^2(V_g - V_t)^2} \quad (5)$$

This is however valid only in strong inversion ($V_g >> V_t$) and linear ($V_{ds} << V_{gs} - V_t$) regime. This approach may be useful in high gate and low drain voltage bias and when α_{sc} can be considered bias-independent, nonetheless in [12] it was shown that what can be considered constant with gate bias is the product $\alpha_{sc}\mu_{eff}$, explaining the use of the factor Ω in (1). Thus for circuit noise simulations, where the continuity from weak to strong inversion and the validity in both linear and saturation regimes are of critical importance, the combination of (1) and (5) is not advised. The authors have demonstrated in [8] that, actually, the measured g_m already accounts for both intrinsic (channel mobility) and extrinsic (access resistance) types of degradation. Therefore, concerning the CNF part ($\Omega = 0$), (1) can be used for circuit noise simulations, independently of the current degradation, provided that g_m is calculated including any access resistance impact (see III. C).

C. Access resistance effect

Regarding the CMF ($\Omega \neq 0$) contribution, it was also proven in [8] that the I_d/g_m term inside the parenthesis of (1) and (3) should only include the mobility attenuation effect, and not the current limitation induced by the presence of the access resistance, R_{sd}. Therefore the generic CNF/CMF model, that includes both intrinsic and extrinsic current degradation effects and is continuous from weak to strong inversion and valid in both linear and saturation regions, is given by (6) [8], where $(I_d/g_m)_0$ represents the value of I_d/g_m when no R_{sd} is present.

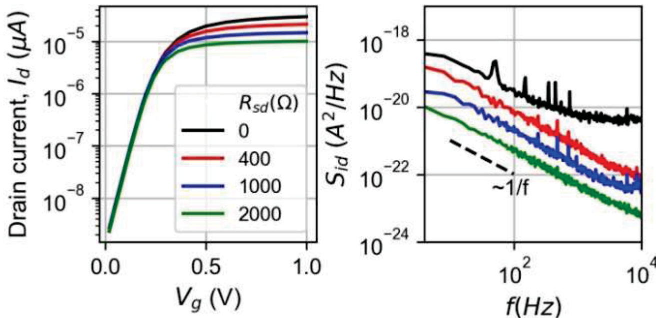

Fig. 1. Measured drain current (left) and noise spectra for $V_g = 0.6$ V (right), for 4 different values of external resistance R_{sd}.

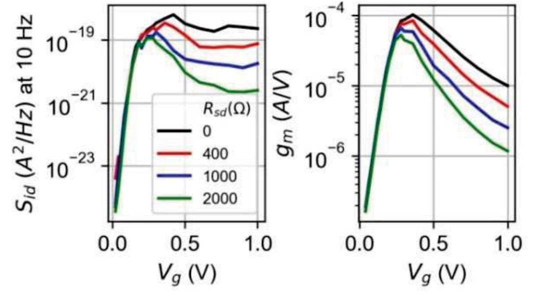

Fig. 2. Measured drain current noise at f = 10 Hz (left) and gate transconductance (right) versus gate voltage for 4 different values of connected external resistance R_{sd}.

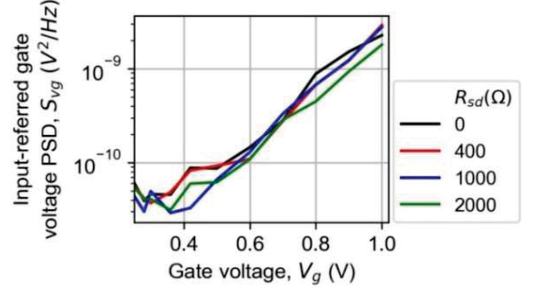

Fig. 3. Measured input-referred gate voltage noise versus gate voltage for 4 different values of connected external resistance R_{sd}.

$$S_{id} = g_m^2 S_{V_{fb}}\left(1 + \Omega\frac{I_d}{g_m}\Big|_0\right)^2 \quad (6)$$

A n-channel FinFET fabricated at IMEC-Leuven, with number of fins N_{fin} = 22 nm, fin height H_{fin} = 26 nm, channel length L = 28 nm and fin width W_{fin} = 4.5 nm was used to demonstrate this effect. The measured results shown in Fig. 1 reveal a 1/f noise level reduction with the -externally connected- R_{sd}, which seems to follow the degradation of I_d in high gate voltage bias. This becomes more apparent when the PSD value at 10 Hz is plotted versus V_g, as in Fig. 2. To verify if this noise level reduction can be entirely attributed to the transconductance degradation (see Fig. 2) due to the proportionality of S_{id} and g_m^2 (1), the S_{Vg} is calculated and plotted in Fig. 3. It is evident that there is no impact of R_{sd} on S_{Vg}, neither in weak nor in strong inversion, despite the presence of CMF, clear from the bias-dependency of S_{Vg}. This finding solidifies the validity of (6) and (3), provided that $(I_d/g_m)_0$ is used instead of I_d/g_m, and these are the formulations used in the Verilog-A modeling presented below.

III. Verilog-A Modeling Methodology

A. Lambert-W (LW) drain current modeling

Since the noise model (6) does not require the use of a specific I_d model, as it is based on measurable quantities of I_d and g_m regardless the model, the Lambert-W (LW) approach, providing a model validated for many advanced CMOS technologies [15], was chosen. Apart from its simplicity to model in Verilog-A, it provides the possibility of direct g_m calculation using a drain current analytical expression and the *ddx* operator. The MOSFET parameters used are: W = 80 nm, L = 30 nm, t_{ox} = 1.55 nm, V_t = 0.3 V.

B. Modeling g_m in the presence of R_{sd}

Although the *ddx* operator can be proven very useful, it can only provide a symbolically-computed partial derivative of the state variable. This would probably not cause any

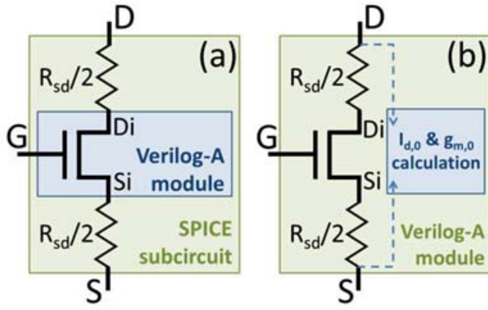

Fig. 4. Access resistance SPICE implementation with a) separate Verilog-A module for the MOSFET and R_{sd} connected inside a subcircuit, b) Verilog-A module including both MOSFET and R_{sd}.

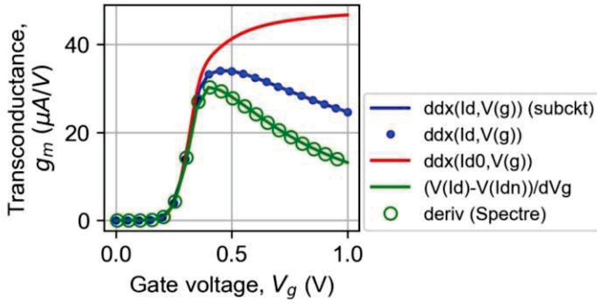

Fig. 5. LW-based simulation of gate transconductance versus gate voltage using four different methods, for R_{sd} = 400 Ω, V_{ds} = 20 mV. The post-simulation calculation in Spectre is shown in circles.

issue when the value of transconductance, g_m, can be calculated directly from a compact I_d expression as a function of V_{gs} and V_{ds}, however the presence of the access resistance, R_{sd}, (Fig. 4) makes this calculation cumbersome, due to the recursive nature of the problem. As expressed in (7), I_d is a function of the internal node voltages $V_{d,i}$ and $V_{s,i}$, which due to R_{sd} are themselves dependent on I_d.

$$\begin{aligned} I_d &= f(V_{ds,i}, V_{gs,i}) \\ V_{ds,i} &= V_{ds} - I_d R_{sd} \\ V_{gs,i} &= V_{gs} - I_d R_{sd}/2 \end{aligned} \tag{7}$$

For the noise source implementation of (1), where the extrinsic (R_{sd}-aware) g_m is needed, a possible implementation method would be to create a sub-circuit where the MOSFET is described through a Verilog-A module which calculates g_m using the *ddx* operator, and R_{sd} is connected in series in two equal parts, as shown in Fig. 4(a). However, as can be seen in Fig. 5, this implementation does not fully account the degradation induced by R_{sd}, which is visible in the post-simulation g_m calculation done in Cadence Spectre.

An alternative approach is to include R_{sd} within the MOSFET Verilog-A module as two additional resistor branches in series with D and S, as in Fig. 4(b):

*V(d,di) = I(d,di)*Rsd/2;   V(si,s) = I(si,s)*Rsd/2;*

At the same time, I_d can be expressed as a function of the internal nodes *"di"* and *"si"* as in (7), so that *ddx(Id,V(g))* includes the voltage drop across R_{sd}. It is reasonable to expect that this method should resolve the calculation issue observed in the subcircuit case; nonetheless Fig. 5 shows that this method gives an identical, yet false result.

A way to properly declare the recursive equation (7) which includes R_{sd} in Verilog-A, is to use a virtual electrical node, (*"id"*) for the drain current definition, whose potential, *V(id)*, is defined by a recursive voltage contribution expression:

*V(id) <+ f (V(d)-V(id)*Rsd ,V(g)-V(id)*Rsd/2) ;*

where *f* is the $I_d(V_{ds,}V_{gs})$ compact model function in which *V(d,s)* has been replaced with *V(d,s)-V(id)*Rsd* and *V(g,s)* with *V(g,s)-V(id)*Rsd/2*. It is important to note that this method can be applied independently of the compact model, as long as I_d is an explicit expression of V_{ds} and V_{gs}. While this approach gives the same result for I_d, it also provides the possibility of accurate R_{sd}-aware g_m calculation, through the creation of a secondary virtual node, *"idn"*, which carries the nearby current, $I_d(V_g\text{-}dV_g)$, calculation for a very small gate voltage bias difference, dV_g = 1mV:

*V(idn) <+ f (V(d)-V(idn)*Rsd ,V(g)-dVg-V(idn)*Rsd/2) ;*

This way g_m can be easily calculated as:

gm = (V(id)-V(idn))/dVg ;

The calculation result of this recursive method is also plotted in Fig. 5, where a perfect agreement with the post-simulation current derivative can be observed, validating its accuracy. To underline the importance of this finding, the BSIM4-SOI [16] model was used to compare the transconductance calculated in the model's Verilog-A code against the post-simulation derivative of I_d in Spectre. Fig. 6 reveals that for a drain/source sheet resistance of R_{sh} = 200Ω/sq, there is one order of magnitude overestimation of g_m by the BSIM model, which incorporates the method shown in Fig. 4(a) for the inclusion of R_{sd}. Therefore it is possible that even some industry-standard models do not accurately account for degradation effects such as the access resistance.

C. Degradation-aware compact noise modeling

The noise in a MOSFET model can be declared either as a voltage noise source, S_{Vg}, in series with G, as illustrated in Fig. 7(a), or as a current power spectral density, S_{id}, in parallel with D and S, as in Fig. 7(b-c). Both BSIM [16] and PSP [17] industry-standard models utilize the S_{id} implementation, and instead of (1) (g_m-based formula) they express S_{id} as a function of I_d. The problem, as already shown, is that this type of implementation cannot properly

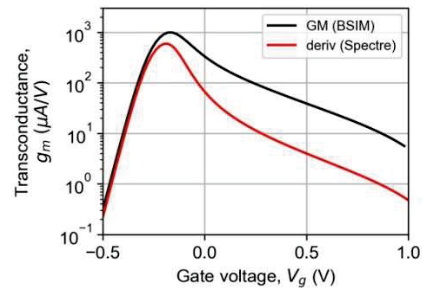

Fig. 6. Simulation of gate transconductance versus gate voltage using the BSIM4-SOI model [16] with R_{sh}=200Ω/sq and t_{ox} = 1.5 nm, V_{ds} = 50 mV. Post-sim calculation in Spectre is shown in red.

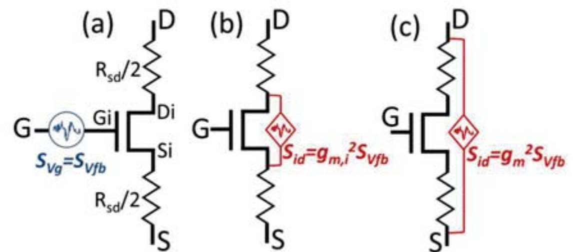

Fig. 7. Flicker noise implementation with a) current noise source in parallel with output and b) voltage noise source in series with V_g.

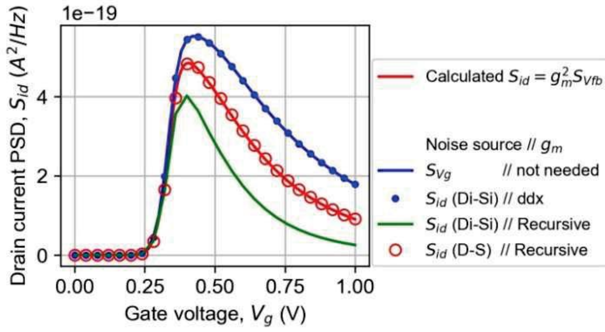

Fig. 8. LW-based simulation of drain current noise at 10 Hz for various noise source implementation methods versus gate voltage (V_{ds} = 20 mV).

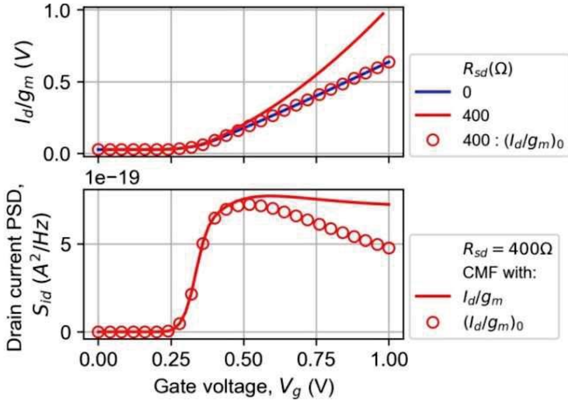

Fig. 9. LW-based simulation of current to transconductance ratio without and with R_{sd} = 400 Ω (top) and drain current noise at 10 Hz with extrinsic and intrinsic CMF calculation for R_{sd} = 400 Ω (bottom) versus gate voltage (V_{ds} = 20 mV).

account neither for intrinsic nor for extrinsic types of current degradation. In particular, it was demonstrated that the R_{sd} impact is challenging to incorporate even when using g_m in the noise expression as shown in Fig. 7(b).

Therefore the S_{Vg} source implementation, as in Fig. 7(a), would reasonably be the best choice for degradation-aware modeling of the CNF model. Nevertheless, Fig. 8 illustrates how a MOSFET's output noise may be overestimated in case it is modeled through S_{Vg} in the presence of access resistance. Same goes for the case where LFN is declared through S_{id} between D_i and S_i as in Fig. 7(b), regardless the way g_m is calculated. The only scenario where the simulated LFN level coincides with the one calculated using the post-simulation g_m values, $S_{id}=g_m^2 S_{Vfb}$, is when the recursive declaration of I_d in Verilog-A for the g_m calculation is combined with the S_{id} source declaration between the external terminals D and S.

Furthermore, considering the CMF contribution, the intrinsic $(I_d/g_m)_0$ has to be calculated within the Verilog-A module. This can be achieved by implementing the idea shown in Fig. 4(b): the $I_{d,0}$ and $g_{m,0}$ are calculated using the external S and D potential values, as if R_{sd} was short-circuited. A validation of this type of calculation is shown in Fig. 9, where $(I_d/g_m)_0$ is evidently equal to I_d/g_m when R_{sd} = 0. If I_d/g_m is used instead, S_{id} in strong inversion can be significantly overestimated in the presence of access resistance.

IV. Conclusion

A compact noise model implementation method that accounts for current degradation effects in nanoscale MOSFETs has been presented. The importance of such effects for noise modeling was demonstrated through measurements and simulations, revealing a significant output noise reduction in the presence of series resistance, which becomes critical in aggressively scaled down (sub-50nm) channel lengths. This effect being directly related to the transistor transconductance, we identified the optimal method of R_{sd}-aware g_m calculation in Verilog-A as the recursive drain current calculation through an internal node, and the correct module positioning: a current noise source in parallel with the external drain/source terminals.

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