Exploring Different Circuit-level Approaches to the Forming of Resistive Random Access Memories

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***Abstract*— Advances in emerging resistive random-access memory (ReRAM) technology show promise to be used in future memory-centric computing systems. In ReRAM arrays that consist of two-terminal bipolar resistive switching (RS) devices, SET/RESET programming voltage pulses are used to switch them from low resistance state (LRS) to high resistance state (HRS). The recent commercialization of discrete and crossbar-array organized RS devices have certainly pushed forward experimentation with such emerging memory technology. One barrier still preventing their widespread practical use is the behavioral variability and the lack of a straightforward manner to implement the forming process and achieve uniform SET/RESET programing. In this paper, different circuit topologies and approaches are explored to perform the forming of the conductive channel in commercial discrete RS devices by Knowm Inc. A target-resistance is pursued through pulsed voltage stress, followed by cycle-to-cycle stabilization using a custom transimpedance amplifier circuit. Moreover, a voltage controlled low–current source is proposed as an approach to alleviate the complexity and risk of the forming process in device characterization.**

***Keywords*— memristor; resistive switching; resistive RAM; ReRAM; characterization; Knowm; conductive channel forming**

I. Introduction

The resistive switching phenomenon in electronic devices has attracted a wide interest from academia and, most recently, from the industry too, due to its application to store information in resistive random-access memories (ReRAM) [1], enabling the development of neuromorphic and memory-centric computing systems [2], [3]. The resistive switching (RS) devices, also usually called memristors [4], basically consist of an insulating layer sandwiched between two metal electrodes [5]. ReRAM devices exhibit memory when operating as two-terminal variable resistors usually due to the formation of a conductive filament (CF) between the top and bottom electrodes, as in the case of conductively bridged (CBRAM) devices. This way, the data stored in ReRAM memory cells are represented by their resistance; for instance, logic '1' by a high resistive state (HRS) and logic '0' by a low resistive state (LRS). In bipolar memristors, one voltage polarity is required to switch the device from HRS to LRS (usually called SET process), and the opposite polarity is required to switch the cell from LRS to HRS (usually called RESET process). The SET operation corresponds to the case when the CF is formed, whereas the RESET describes the process when the CF is dissolved [6], [7].

ReRAM device technology is continuously maturing. *Knowm Inc.* company has released commercially available discrete and crossbar-organized memristors [8], whereas other companies around the world are pushing forward the ReRAM nanofabrication [9], [10]. Robust handling of RS devices with high switching uniformity and analog (multi-level) programmability, are much desired properties for commercial applications. In this sense, one barrier for the widespread practical use of RS devices is the behavioral variability and the lack of a straightforward manner to perform the initial forming process, as well as achieve uniform SET/RESET programing, especially for non-experienced end users. Being able to use the same pulsing procedure to stably program a device several times to its HRS and LRS state would highly benefit the design and development of circuits for ReRAM applications, also facilitating future reproducibility of research results based on commercially available ReRAM devices. In this sense, the initial forming process to take place on pristine RS devices has attracted a great interest due to its influence on fundamental and engineering parameters such as conductivity [6], cycling repeatability [7], consumption [11], multistage response [12] or frequency response [13].

Despite such importance, there is yet to be defined a common procedure for the forming stage of ReRAM devices. In relevant works we usually observe that a compliance current is set-up in instrumentation equipment [6], [7] which however is electronically complicated to implement in ReRAM driving circuitry at application level. Others recommend using a high series resistor to protect the device while applying a voltage ramp that might reach much higher voltages than usual operating voltages for SET/RESET. This, however, creates a voltage divider whose impact on the quality of the forming process is difficult to control [14].

In this context, we explore different circuit topologies for device measurements and approaches to achieve the initial forming process. We present a ReRAM forming strategy based on the definition a target resistance to be achieved by the application of pulse trains of gradually increasing amplitude. Moreover, we suggest a current-driven characterization strategy for memristors which practically eliminates the risks and complexity of the forming process. To show the feasibility of such strategies, measurements were carried out on RS devices developed and commercialized in 16-pin ceramic DIP package by *Knowm Inc.*, using a custom circuit associated to basic control lab equipment [15].

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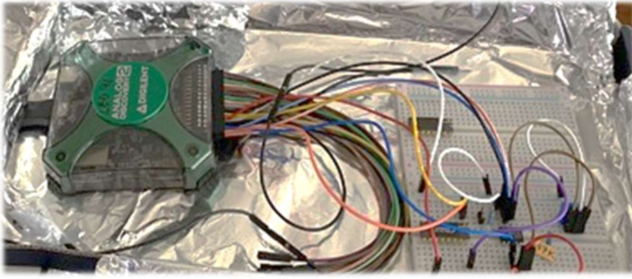
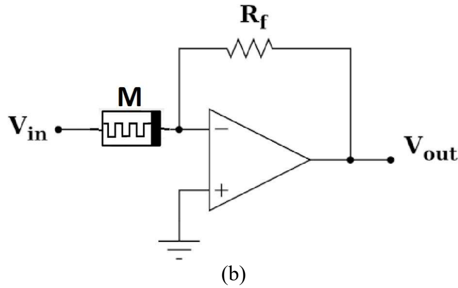


(a)



(b)

Fig. 1 (a) Schematic of the circuit implementing a transimpedance amplifier, used for measurements. M is the RS device under test, whereas R_f is a feedback resistor whose value was selected close to the target resistance value for the RS device during forming. (b) Custom experimental setup.

II. Experimental Setup

Measurements were carried out using the digital oscilloscope and the function generator of the Digilent Analog Discovery 2 (AD2) instrumentation tool [15] and custom circuits. Part of the experimental setup is shown in Fig. 1(a). As far as RS devices are concerned, we used commercial self-directed-channel (SDC) bipolar RS devices by *Knowm Inc.* [8], [14]. SDC devices constitute an ion-conducting device type, a sub-class of electrochemical metallization devices which, in response to an applied voltage, use a metal-catalyzed reaction within the device active layer to generate conductive channels (Ag ion transport routes) that contain Ag agglomeration sites, permanent under similar operating conditions.

One of the circuits we used was a transimpedance amplifier where the bottom electrode of the RS device under test was permanently connected to the inverting input of an operational amplifier, as shown in Fig. 1(b). Such circuit is a current-to-voltage converter, allowing to transform the current flowing through the ReRAM device into a voltage measured at its output V_{out}. At the same time, the applied voltage on the device is always V_{in}, owing to the virtual ground node where the bottom electrode of the device is connected. The AD2 instrument was used to supply the desired voltage V_{in} and to measure V_{out} on the output node of a LT1357 operational amplifier (opamp), used due to its high speed and high slew rate. The offset of the opamp was properly compensated in hardware. On the other hand, we also used a voltage-controlled low-current source topology, originally proposed in [16] and later used in different contexts [17]. Such circuit allows to continuously monitor the voltage drop on the device, while at the same time it drives a stable current in the pico-/nano-ampere range through the RS device, which is independent of its resistance of the device. For its implementation we used the ADTL082 operational amplifier due to its high speed, high slew rate, and also very low input bias current and voltage, with external ±12V supply voltage.

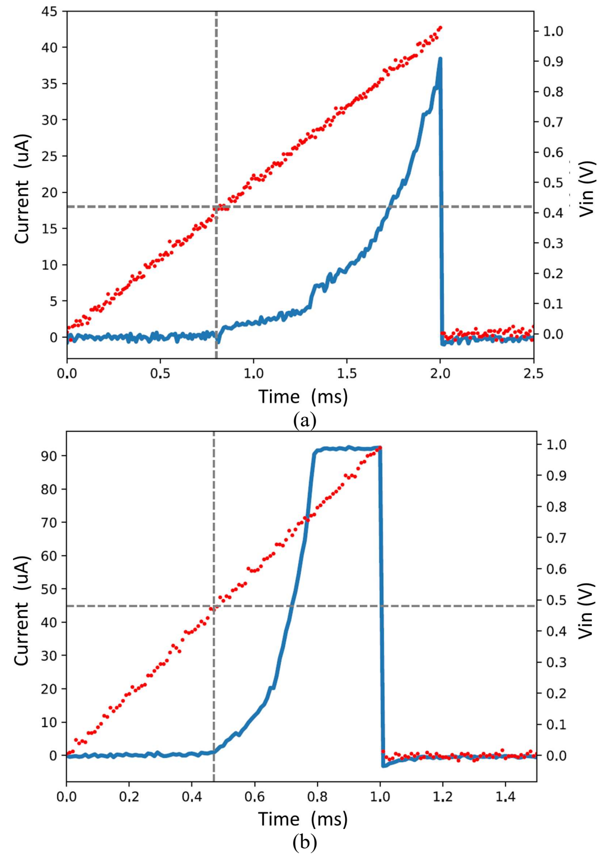


Fig. 2 Measured data of forming process using the transimpedance amplifier topology and a voltage ramp which reached to 1V at (a) 2ms and (b) 1ms. Red curve corresponds to applied voltage Vin. Blue curve corresponds to current through the device, computed via the measured Vout voltage. Gray dashed lines indicate the moment when SET process initiated.

Besides the Waveforms Software, typically suggested to work with all portable Digilent instruments, we developed an ad-hoc graphical user interface (GUI) in Python using the Digilent SDK, to facilitate operation and control of the specific measurements required for RS devices and control of the custom circuit topologies. The GUI supports different types of sequences of configurable voltage pulses, such as consecutive pulses, voltage sweep, forming process, unsymmetrical voltage ramps for current-voltage hysteresis, and individual pulses for exploration of RS behavior. In all cases GUI allows parametric input voltage design and previsualization of the input signal, realization of experiment and visualization of measured data including the calculation of the resistance of the device.

III. Results and Discussion

The initial forming process to take place on pristine RS devices is essential, thus it is important to figure out methods and circuits that allow such process to be implemented at application level. The following experiments concern the use of transimpedance amplifier as basic circuit topology. We observe the variability of the forming process in the results shown in Fig. 2(a) and Fig. 2(b), which present the evolution of the forming of different BS-AF-W discrete SDC bipolar RS devices by *Knowm Inc.* We notice the difference in the time scale of the applied rising ramp voltage required to produce the same current through these two different devices. Particularly, we observe that in Fig. 2(b) the applied voltage caused the saturation of LT1357, protecting the device under test from damage by limiting the current at ≈90uA.

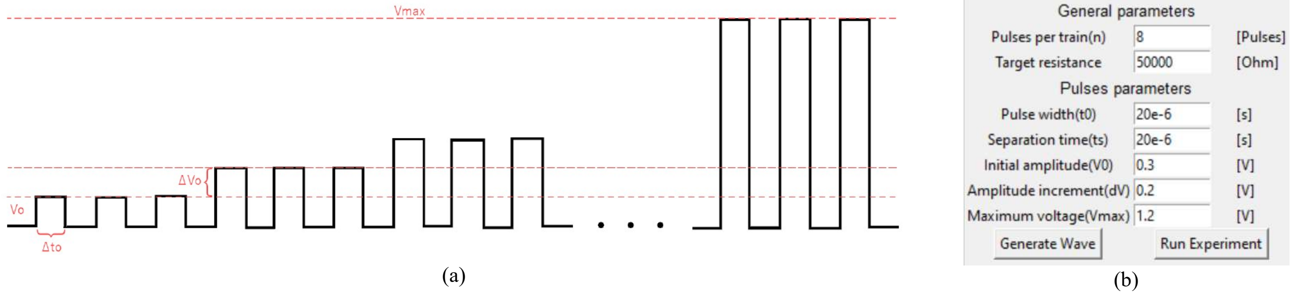


Fig. 3 (a) Diagram showing the general description of the pulse train applied to the RS device during the forming process. (b) Configuration example for a forming experiment through the GUI designed for AD2 control and experiment configuration.

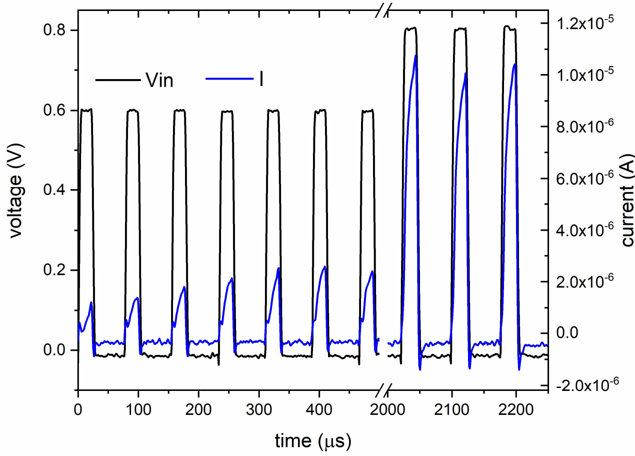


Fig. 4 Experimental measurements showing the current while focusing on the first and the very last applied pulses during the forming process.

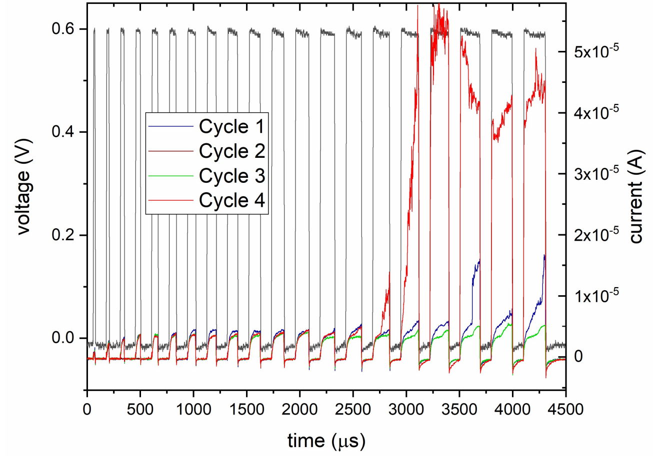


Fig. 5. Experimental measurements showing consecutive cycles of square 0.6V-pulses whose time-width increased from 10 to 200μs.

There is generally un uncertainty about the correct amplitude and duration of the ramp or any pulse signal to be applied to a pristine RS device to achieve forming. For this reason, we designed an experiment which consists in applying an exploratory train of pulse groups of different characteristics until a desired user-defined target resistance has been reached. An example of the configuration of a pulse train designed for the forming process is shown in Fig. 3(a), whereas Fig. 3(b) shows the configuration options available through the GUI for this particular experiment. All pulses have the same duration (t0). The user defines the number of pulses in each group, the starting amplitude (V0) and a desired amplitude increment (dV) between consecutive pulse groups. The same applies when the amplitude is kept the same and the pulse-width is incremented. The idea behind this incremental voltage stressing is to gradually modify the applied pulse characteristics until forming is achieved. The experiment will stop after any pulse if the user-defined target resistance has been reached, or will continue until the maximum pulse amplitude (Vmax) of the maximum pulse-width is exceeded. If forming was not achieved, we repeat the process for an increased number of pulses, or for an increased pulse-width or a higher maximum voltage limit (Vmax).

Following the descriptions provided in Fig. 3, sequences of pulses of increasing amplitude up to 0.8V were applied to a pristine device. Similar to other relevant works [11], [19], voltage pulses in the order of several microseconds were used. The GUI was setup to stop the experiment once a target resistance of 50kΩ were achieved. As it can be observed in Fig. 4, the evolution of the current response is clearly different in first pulses than in the last ones. Despite this response is clear, current does not immediately follow voltage as in other works [11], [19]. The implementation of such short-time forming cycles could be compatible with the high frequency response of devices described elsewhere [13]. To investigate this possible effect, pulses of increasing time-width for a constant voltage amplitude were used. Figure 5 depicts four such cycles of 0.6V square pulses of gradually increasing time width from 10 to 200μs. It is interesting to observe the different behavior of the current for short and for wide voltage pulses. While for pulses of up to ~100μs the device behaves in a way similar to what was observed in Fig. 4, for wider pulses we observed ~5 times more current. These results are compatible with pulsed voltage stress (PVS) described recently in [19]. Physically, cycles define the formation of the conductive channel and therefore the device RS performance.

Next, in order to test the SET/RESET operation, two double unsymmetrical triangular pulses from 0.6V (SET) to -0.2V (RESET) in 130μs (entire double ramp) were repeated more than one hundred times on the recently formed device. The asymmetry in the positive and negative ramps is due to the asymmetry in the SET and RESET voltage thresholds that the SDC devices have. As shown in Fig. 6, even after the forming (see Fig. 4) and the voltage stress (see Fig. 5), the device under test does not exhibit repeatability in the first ramps. Such lack of repeatability in the first pulses results in a lack of memory capability in the device, attributed to the recent formation of the conductive channel. After ~20 SET/RESET cycles, the RS performance shows high repeatability. This can be also noticed in Fig. 7 which shows the evolution of the current measured at 0.5V after every

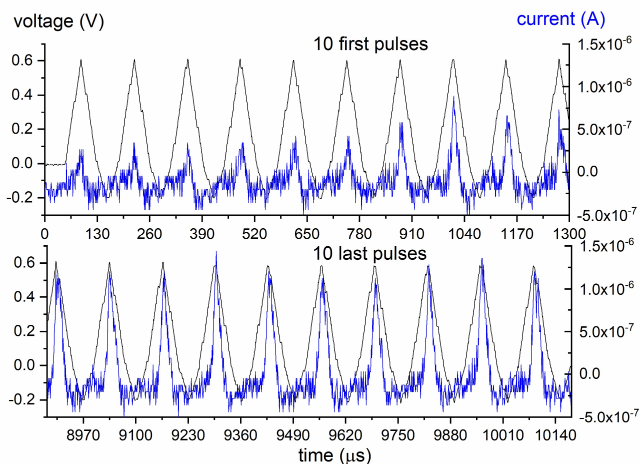


Fig. 6. Results showing the current evolution for unsymmetrical positive-negative ramp voltage for SET (0.6V) and RESET (-0.2V). The plots focus on the first 10 and the very last 10 ramps.

SET/RESET cycle in Fig. 6. Resistance window is improved and, besides variability, switching performance is more stable and repeatable, indicating the expected memory performance. Finally, totally different results are obtained when the device is driven by a current source. Figure 8 presents the *i-v* curves obtained for 200us-wide triangular current pulses up to 500nA for SET and -100nA for RESET. The forming process was not a separate required process; the conductive channel was immediately formed at the very first applied current pulse. More stable cycling performance can be also observed.

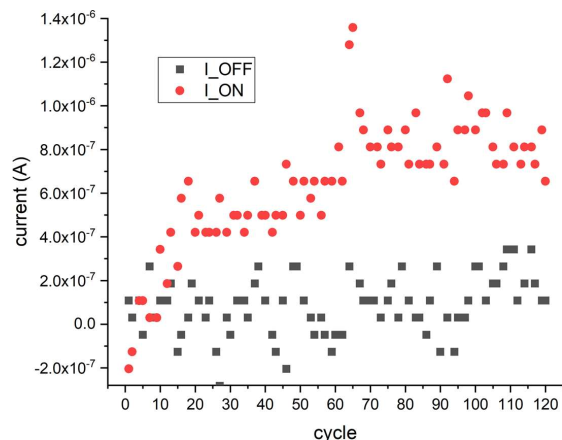


Fig. 7. Results showing the current evolution during the application of the unsymmetrical positive-negative ramp voltages of Fig. 6.

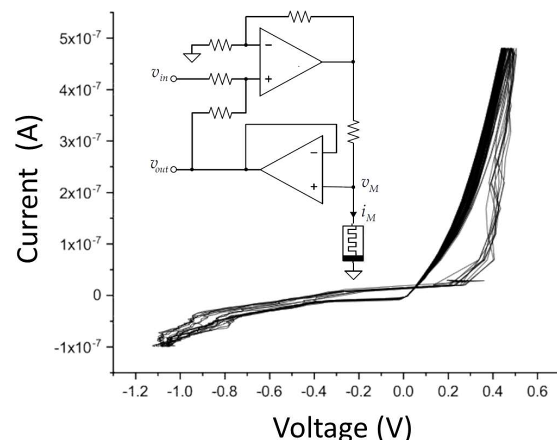


Fig. 8. Current-voltage curves from a current-driven device. The inset shows the implemented topology of a voltage-controlled current source.

IV. Conclusions

This paper showed that the gradually increasing pulsed input for a specific target resistance is an effective and easy to implement forming strategy. After forming, a set of a few hundreds of SET/RESET cycles lead to further stabilization of resistive switching and a wider HRS-LRS resistance window. Current-driven ReRAM devices exhibited an improved hysteresis performance and stable cycling. Future work will explore repeatability of performance in different device types and packages for thousands of cycles towards the formulation of a laboratory tutorial for safe handling of RS devices.

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