Digital Control Implementation for PV Cell-Level Inverters

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***Abstract*—This paper presents the design procedure of the digital control unit of an on-chip photovoltaic (PV) cell-level DC/AC inverter. Its main blocks are presented, along with their interconnections and timing, whereas the state diagram, based on the sinusoidal pulse width modulation (SPWM) is given, for both grid-tied and standalone operation. The proposed digital control unit is experimentally validated in a laboratory test bench, comprising four full-bridge (H-bridge) inverters in cascaded configuration. The TMS320F28379D microcontroller is employed, as it is suitable for such applications. Finally, experimental results indicate the operational characteristics of the proposed digital control scheme, being the first step for on-chip integration.**

Keywords—microcontroller, H-bridge inverter, on-chip converter, PV cell, PV inverter

I. Introduction

In both large-scale photovoltaic (PV) plants and small-scale residential PV installations with conventional inverter types (e.g., transformerless string inverters or microinverters), the energy yield may be reduced, as a consequence of mismatch losses among PV cells. Two critical causes of energy reduction are the partial shading, especially in building-integrated PVs and the potential induced degradation (PID) effect [1].

Hence, PV cell-level inverters constitute a current and future trend, in order to overcome the aforementioned problems and maximize PV system efficiency. The AC cell inverter system has been presented and investigated within the framework of the *"SmartPV"* project and it is the case where each individual PV cell is connected to a DC/AC converter. The most challenging issue is the design of a highly-efficient on-chip power converter (both in terms of topology and control / synchronization strategy), capable to amplify very low voltages up to an appropriate level for the utility grid [2], [3].

Under this light, this work aims to present the basic design steps of the digital control unit of the on-chip PV cell-level inverter. The main controller blocks are presented and discussed along with their interconnections and timing (sequence of events). Next, the state diagram is developed for sinusoidal pulse width modulation (SPWM) considering grid-tied as well as standalone operation. The most critical points of the design process (i.e. requirements, considerations and limitations) are highlighted and discussed. The proposed digital control unit is validated in a laboratory test bench of four H-bridge inverters (identical inverters, designed and constructed with discrete components for validation purposes), in cascaded configuration [4].

As regards the digital controller implementation, a TMS320F28379D microcontroller unit (MCU) is utilized, for all H-bridge inverters. The specific MCU is appropriate for power electronics applications, as it holds the necessary hardware / computational resources to drive such a large number of semiconductor switches [5], [6]. Last but not least, experimental results are presented, indicating the operational features of the proposed digital control architecture being the first step for on-chip implementation.

The remainder of this paper is organized as follows; in **Section II** the SPWM-based control system is described in detail, whereas in **Section III** its digital MCU implementation is presented. Following, in **Section IV** the design and construction of the experimental test-bench, comprising four cascaded H-bridge inverters, is described. Finally, the experimental results are presented and discussed in **Section V**, whereas **Section VI** concludes the paper.

II. Proposed System Description

According to [2] and [3] the most appropriate solution for a PV cell-level inverter, in terms of efficiency, robustness, cost-effectiveness and simple control, is a dual-stage DC-AC power conversion system. For the DC-DC and the DC-AC power stages, the synchronous boost and the H-bridge topologies have been selected, accordingly. The synchronous boost converter operates under maximum power point tracking (MPPT) control, harvesting maximum energy from each PV cell and feeds the H-bridge inverter. The latter one is responsible for power transfer to the utility grid, synchronization and stabilization of the DC-link voltage. In order the output of the PV system to be in an appropriate level for grid-tied operation, the outputs of all PV cell-level inverters are connected in cascaded configuration.

In this work, the H-bridge digital control implementation, which is based on the well-established SPWM scheme, will be presented and discussed, for both grid-tied and standalone operation. **Fig. 1** illustrates a schematic diagram of the studied system, comprising four cascaded H-bridges, which is valid for the experimental test bench as well. In addition, **Fig. 2** depicts the SPWM-based controller block diagram for standalone and grid-tied operation, respectively.

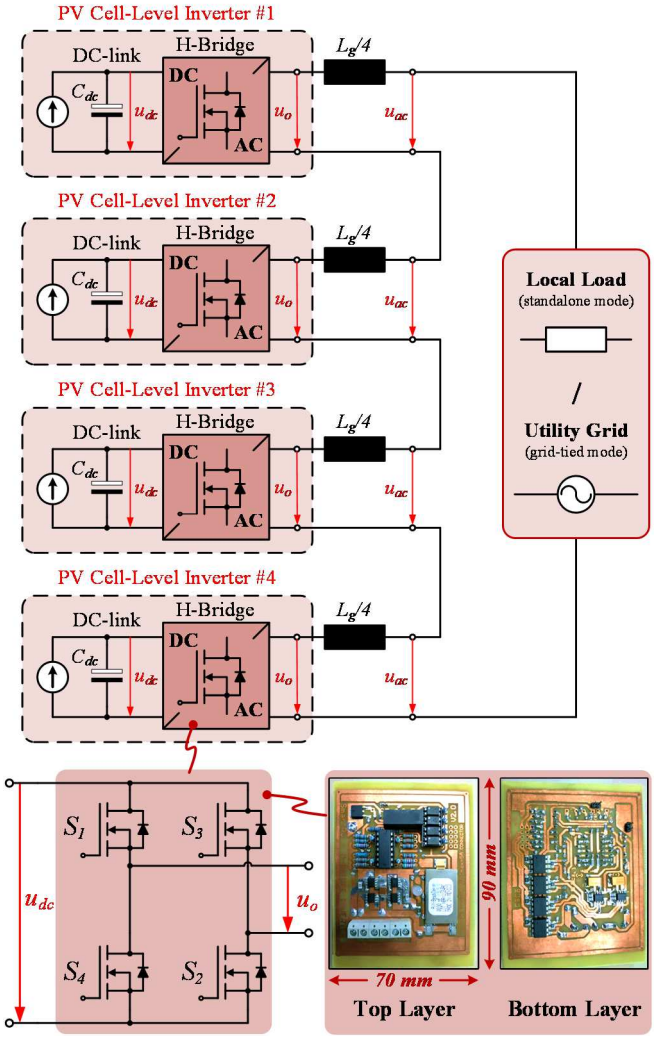

Fig. 1. Schematic diagram of the studied system, comprising four PV cell-level inverters, along with the experimental implementation of each H-bridge module.

The bipolar SPWM technique is implemented as in [4]. At first, the DC-link voltage (u_{dc}) is compared with a reference voltage ($u_{dc,ref}$) and the error is fed to a proportional-integral (PI) controller. The PI output determines the modulation index (m_a) of the SPWM, multiplied then with a sine wave. Depending on the inverter operating mode (standalone or grid-tied), the sine wave is derived either internally (by software), or generated by the measured grid voltage in each H-bridge output (u_{ac}), via a Phase-Locked Loop (PLL). It is worth noting that the output filter inductance (L_g), necessary for grid-tied operation is divided and shared among each H-bridge output ($L_g/4$), so as to effectively measure the grid voltage in each inverter output. The PLL is synchronized with u_{ac}, providing a synchronous reference signal for the SPWM unit. Last but not least, the grid fundamental angle (θ_b) is subtracted by a constant value ($\Delta\theta$), introducing the appropriate phase difference between the H-bridge output and the utility grid voltages.

In each H-bridge module, u_{dc} and u_o are measured and fed to a signal conditioning circuit comprising operational amplifiers, for the appropriate gain and DC offset calibration. Then, the signals are fed to the ADC module of the MCU, for sampling and digital processing. In the final experimental implementation, u_o of the first (#1) H-bridge is measured and processed, using a common, digitally implemented PLL. Thus, grid frequency and phase angle are extracted, determining the frequency and phase angle of the SPWM modulation signals. Moreover, u_{dc} is compared to a fixed reference value (i.e., 3 V in the developed system) and processed by the aid of a digital PI controller. The PI output is actually the m_a value, resulting in the effective regulation of the DC-link voltage at the desired level. Finally, for standalone operation, an internal software-generated 50 Hz sine wave is used, instead of the grid voltage signal (u_{ac}).

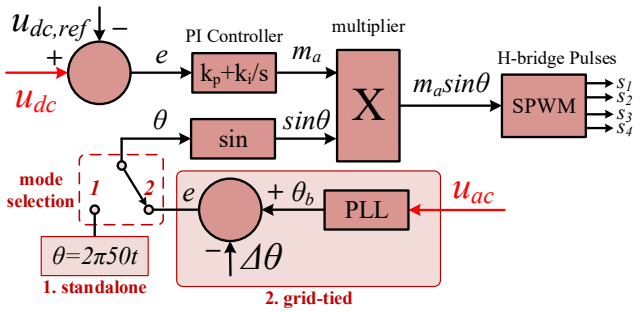

Fig. 2. Block diagram of the SPWM-based controller, for standalone and grid-tied operation.

III. Digital Implementation

For the digital control implementation, a LAUNCHXL-F28379D (C2000 Delfino) development board by Texas Instruments, equipped with the TMS320F28379D MCU is employed [7]. The specific MCU controls all H-bridges in the experimental setup. The block diagram of the controller hardware implementation is presented in **Fig. 3**.

The "Time-Base Counter" submodule, of the enhanced pulse width modulation (ePWM) module increments the CTR register from 0 up to the PRD value. By setting this counter to "Up" mode, once the CTR value reaches PRD, the counting starts over from 0, creating a positive slope sawtooth waveform. With a fixed prescaler value and by varying the PRD value appropriately, the sawtooth waveform frequency is derived (i.e., 50 kHz in this work). In addition, the "Time-Base Counter" (along with the "Counter Compare" submodule) generates three control commands, depending on the CTR value (i.e., CTR = 0, PRD, CMPA). In this way, the CMPA register value (set by software) defines the PWM signals duty cycle value.

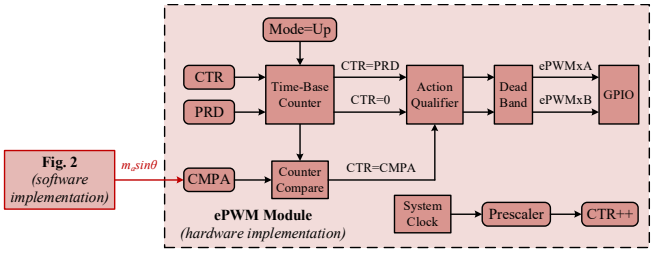

Fig. 3. Digital control hardware implementation (ePWM module), by the aid of the TMS320F28379D microcontroller.

The above mentioned control signals are then fed to the "Action Qualifier" submodule that determines the time intervals at which the output signal is either "high" or "low". Specifically, output A becomes "high" when CTR=CMPA in ascending count and "low" when CTR=PRD, whereas output B receives the opposite value (B= $\overline{A}$), generating two

complementary pulses to drive the high-side and low-side switches (power MOSFETs) of each H-bridge leg. Finally, the "Dead-Band" submodule is utilized to introduce the necessary delays between the ePWMxA and ePWMxB signals, for safe MOSFET driving.

Last but not least, in order to generate the SPWM waveform, the duty cycle value must follow a sinusoidal waveform, which is produced using the PLL unit described above. A fixed phase difference ($\Delta\theta$) is subtracted from the PLL angle, so as to achieve the desired active power transfer to the AC grid (in relation to the L_g value), in grid-tied operation. Finally, the CMPA register value is calculated, based on the generated sine waveform ($\theta=\theta_b-\Delta\theta$), resulting in the SPWM output. The flowchart of the developed control scheme (described in detail in **Sections II** and **III**) is illustrated in **Fig. 4**.

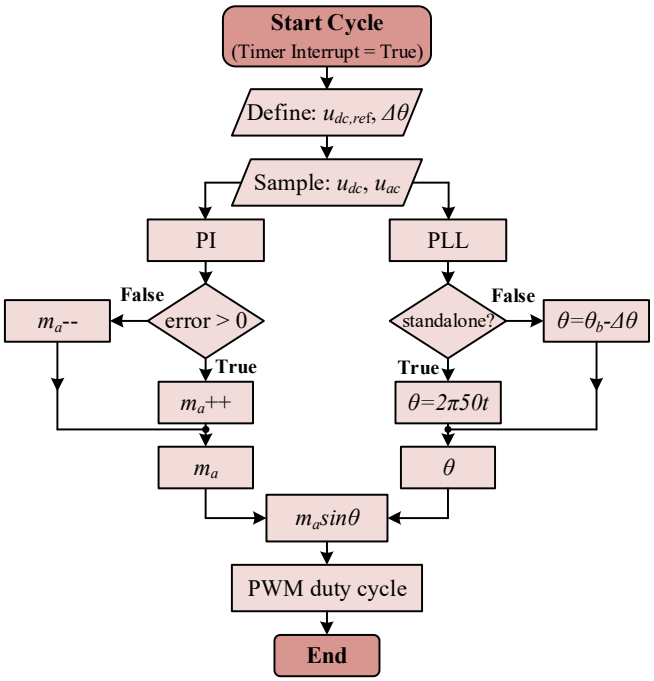

Fig. 4. Flowchart of the developed control scheme.

IV. Experimental Setup

The developed laboratory experimental test bench is according to **Fig. 1** and comprises four cascaded H-bridges, each one designed and constructed with discrete semiconductor devices. Miniature sized surface-mount (SMD) components are selected, in order to come up with a very compact design, minimizing distances, and thus the parasitic inductances between components. The main components and parameters of the experimental setup are listed in **Table I**.

In addition, in order to achieve the required DC voltage regulation at the DC-link, the parallel combination of an SMD supercapacitor and a ceramic capacitor (C_{dc}), listed in Table I is utilized. Apparently, a quite high capacitance value is required for smoothing the low voltages of this application. Moreover, for the $S_1 - S_4$ driving, the NCP81075 has been selected, as it is based on the commonly used bootstrap supply technique [5] (incorporating the bootstrap diode), which is considered the most appropriate driver in terms of cost and complexity. Finally, it is worth noting that the MPPT-controlled synchronous boost DC-DC converter is emulated by a DC power supply in constant current mode (i.e., controlled current source).

TABLE I. Experimental Setup Components and Parameters

Parameter / Component	Description / Value
Nominal DC-link voltage (u_{dc})	3 V
AC grid RMS voltage ($u_{grid,rms}$)	7.85 V *(7.85 V /230 V transformer)*
SPWM carrier frequency ($f_{carrier}$)	50 kHz
Semiconductor switches ($S_1 - S_4$)	FDS6680AS power MOSFET with integrated Schottky diode *(30 V, 11.5 A, $R_{DS(on),max}$ = 10 mΩ @ V_{GS} = 10 V)*
Bootstrap driver	NCP81075 dual MOSFET gate driver with on-chip bootstrap diode
Optocoupler	6N137 high speed single-channel optocoupler
H-bridge output inductor ($L_g/4$)	500 μH *(custom, comprising 2xE42/21/15 ferrite cores)*
DC-link capacitor (C_{dc})	30 mF *(*BZ015B303ZSB *supercapacitor in parallel with* C1210C104J5GACTU *ceramic capacitor, total ESR = 192 mΩ)*
Signal (u_{dc}, u_o) conditioning	LM358 low-power dual operational amplifier
Auxiliary power supplies	TMA 1515S isolated DC-DC and LM7805 linear fixed-voltage regulator
Microcontroller unit	TMS320F28379D *(LAUNCHXL-F28379D development board)*

As for the measurement and signal conditioning circuit, for u_{dc}, u_{ac} signals sensing, the LM358 operational amplifier in differential configuration is employed. The necessary isolation is achieved by utilizing optocouplers, both for measurements and driving. In addition, for grid-tied mode a transformer is used to adjust the utility grid voltage down to 7.85 V_{rms}, which is suitable for the developed four H-bridge system with 3 V DC-link per cell. Finally, in order to provide a current limit before synchronization is established, a 10 Ω resistor is connected in series. The resistor is bypassed via a power switch, after synchronization occurs.

V. Experimental Results and Discussion

Indicative experimental results for grid-tied operation are presented in this Section. The objectives of the experiments that are carried out are: (a) to effectively establish the synchronization of each H-bridge output voltage with the utility grid voltage, via the digitally implemented PLL, and (b) to effectively regulate the power transferred to the grid and stabilize the DC-link voltage at the desired value, by the aid of the PI controller.

Each H-bridge is supplied by a constant current source, set at a fixed value, emulating the MPPT-controlled synchronous boost converter, whereas the DC-link voltage reference ($u_{dc,ref}$) is set at 3 V. The phase difference with the utility grid voltage ($\Delta\theta$) is set at a desired value, in order to transfer active power from the inverter to the grid, whereas the amount of active power is defined by the modulation index (m_a).

In **Figs. 5-7** the grid voltage and the inverter output current are depicted, for the case where the phase difference ($\Delta\theta$) between the grid and the inverter output voltage has been set to 15°, 20° and 25°, respectively. For the latter cases, the input current reference is set at 0.6 A, 0.8 A and 1 A, respectively. In all those cases, the synchronization with the utility grid has been established successfully. Moreover, in **Table II**, the measured values of input / output currents and DC-link voltage, as well as the calculated active power are provided, for the three aforementioned cases. Apparently, the higher the

phase difference (within specific limits), the more active power is transferred to the utility grid.

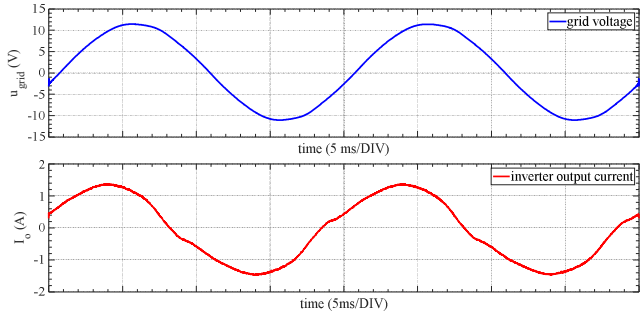

Fig. 5. Grid voltage (blue waveform) and inverter output current (red waveform) for $\Delta\theta$=15°.

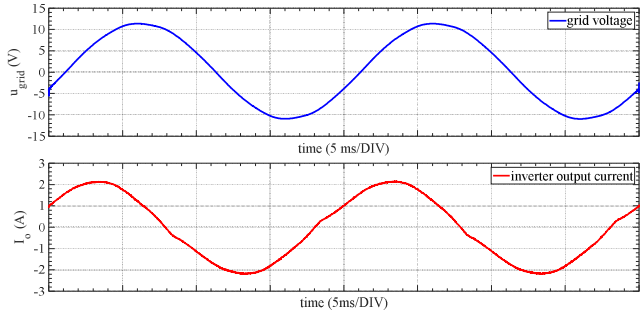

Fig. 6. Grid voltage (blue waveform) and inverter output current (red waveform) for $\Delta\theta$=20°.

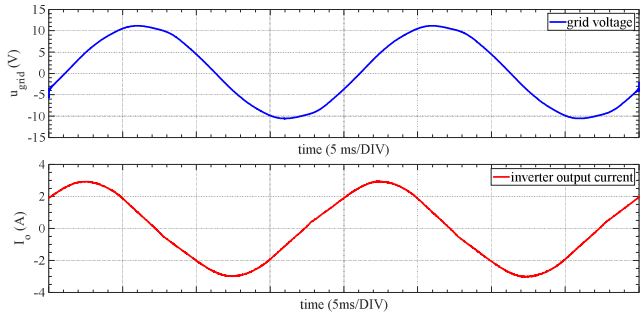

Fig. 7. Grid voltage (blue waveform) and inverter output current (red waveform) for $\Delta\theta$=25°.

As it can be also concluded by **Table II**, the DC-link voltage (u_{dc}) in each H-bridge is effectively regulated at the desired value, through the four independent PI controllers. Thus, the modulation index (m_a) of each H-bridge acquires an appropriate value, so as its output power to be maximized. Therefore, the maximum amount of generated power is injected to the grid.

TABLE II. EXPERIMENTAL MEASUREMENTS

Δθ=15°, I_o = 0.9 A, P = 8.13 W				
	H-bridge #1	*H-bridge #2*	*H-bridge #3*	*H-bridge #4*
u_{dc} (V)	3.21	3.17	3.26	3.23
I_{in} (A)	0.63	0.65	0.63	0.62
Δθ=20°, I_o = 1.4 A, P = 10.52 W				
	H-bridge #1	*H-bridge #2*	*H-bridge #3*	*H-bridge #4*
u_{dc} (V)	3.15	3.10	3.20	3.15
I_{in} (A)	0.83	0.83	0.82	0.85
Δθ=25°, I_o = 1.9 A, P = 11.90 W				
	H-bridge #1	*H-bridge #2*	*H-bridge #3*	*H-bridge #4*
u_{dc} (V)	2.95	2.90	3.05	3.02
I_{in} (A)	1.02	1.03	1.00	1.02

VI. CONCLUSION

In this work the design steps for a digital controller, applicable to a PV cell-level inverter are presented. The SPWM-based controller MCU implementation is experimentally validated in a scaled-down laboratory test bench, comprising four H-bridges in grid-tied mode. The experimental results indicate the functionality and good performance of the proposed controller, enabling its on-chip implementation.

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