Hardware Aspects of Iterative Receivers for V2X Applications

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***Abstract*—In this paper we propose an iterative receiver architecture. The proposed architecture estimates the channel using a weighted function which combines both the coefficients estimated by the known pilot sequence and the decoded bit stream. This approach grants a performance boost of 1.5–2 dB in low bit error rates with the trade-off of more hardware resources utilized. A second, more complex architecture has been evaluated, but discarded as it does not produce any noticeable benefit.**

I. Introduction

Intelligent Transport Systems (ITS) consist of Vehicle-to-Vehicle (V2V) and Vehicle-to-Infrastructure (V2I) communications. Dedicated Short Range Communications (DSRC) is a short range service supporting road safety and traffic efficiency applications, requiring low latency and high accuracy. The physical layer (PHY) specification, relies on IEEE 802.11p, an amendment to the IEEE 802.11 standard that adds wireless access to mobile environments.

IEEE 802.11p uses Orthogonal Frequency Division Multiplexing (OFDM) as its modulation format. Phase-shift keying (PSK) or Quadrature Amplitude Modulation (QAM) can be used, allowing a high data rate. A long symbol and guard interval duration minimizes the effect of inter-symbol interference. A channel spacing of 10 MHz provides a better protection against long delay spreads. A block diagram of an IEEE 802.11p transmitter is shown in Fig. 1 and a corresponding receiver is shown in Fig. 2.

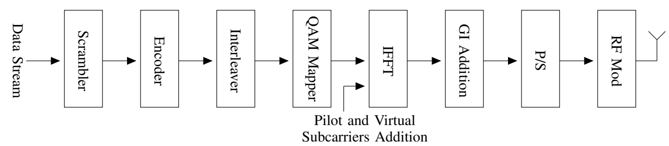

Fig. 1. OFDM Transmitter block diagram

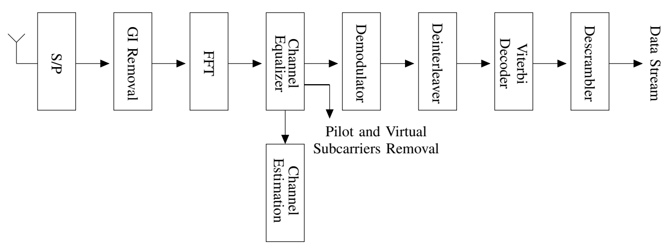

Fig. 2. OFDM Receiver block diagram

The standard specifies the use of training data, originally intended for static devices and indoor use. In the vehicular environment, the high vehicular velocities, the dynamic environment and the long packet sizes mean that the channel cannot be considered static anymore within one OFDM frame. To address this challenge, iterative schemes have been proposed: the decoded data are fed back into the receiver and act as the known training sequence for the subsequent OFDM symbol.

Following the iterative receiver paradigm, the proposed system uses the received data to update the channel estimation at the receiver in the decision directed sense. After the signal is decoded, it is reconstructed to re-produce the transmitted signal $X_{n,k}$, which can be compared to the received information $Y_{n,k}$. Assuming perfect decoding and symbol duplication, the decoded bit sequence can be treated as a regular training sequence and the channel coefficients can be computed using the traditional techniques.

The main drawback of a traditional decision directed channel estimation algorithm, is the error propagation caused by incorrect detected symbols. Several studies have focused on reducing the symbol error propagation effects by estimating detection errors or by providing highly reliable symbols to the channel estimator. Kalyani and Giridhar proposed a system of M estimators, mitigating the error propagation, using a cost function to downweight the incorrect symbols with higher error [1]. Siti *et al.* presented a low-complexity algorithm, using for channel estimation task data subset with the highest expected signal-to-noise ratio [2]. Abdulhamid *et al.* introduced a forgetting factor γ into the recursive channel update equation [3]. Yuan and He present a similar approach in the MMSE sense, extended by a method that detects momentarily distorted by noise subchannels [4]. Kella proposed a delay of M OFDM symbols in order to ensure the convergence of the decoded stream, introducing a delay in the symbol duplication loop [5]. Baek and Lee developed a state feedback decision algorithm that can extract reliable data pilots within a few received symbols without the aid of conventional decoders to minimize the error propagation effect [6]. Han *et al.* proposed an Euclidean distance based reliability test method to reduce the rate of erroneous data pilots [7]. Zhang *et al.* used a threshold value σ, in order to select reliable data symbols for updating the channel information [8].

The remainder of the paper is organised as follows: Section II describes the employed channel and system models. Section III introduces two iterative receiver architectures for evaluation. Section IV presents the simulation results. Sec-

TABLE I
SIX TDL CHANNEL MODELS AND THEIR PARAMETERS

Scenario	Average PER Result (%)
V2V - Expressway Oncoming	5.6
V2V - Urban Canyon Oncoming	4.4
RTV - Suburban Street	3.0
RTV - Expressway	2.7
V2V - Expressway Same Direction with Wall	1.9
RTV - Urban Canyon	0.8

tion V analyses the complexity of the introduced models. Section VI concludes the paper.

II. Channel and System Model

Vehicular communication channel models need to deal with specific characteristics: Diverse environments, combinations of different communication types such as vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I), and both static and mobile objects that affect the communication.

Six time- and frequency-selective empirical channel models for vehicular wireless LANs are presented by Acosta-Marum and Ingram [9]. The tapped delay line model is used, where each tap process is described as having Rician or Rayleigh fading and by a Doppler power spectral density. Each path is parameterized by the Doppler PSD shape, the shape's width, center frequency, excess delay and path power. A composite tap PSD is crafted by assigning several paths with different shapes to have approximately the same excess delay. A brief summary of the six scenarios and their measurement parameters are summarized in Table I.

IEEE 802.11p operates in the f_c = 5.9 GHz carrier frequency band, with 10 MHz sampling frequency. Employs the bit-interleaved coded OFDM technology with 64-point fast-fourier transform (FFT). One OFDM symbol has a symbol duration of T_s = 6.4 μs, and a guard interval (GI) of T_{GI} = 1.6 μs employed to minimize inter-symbol interference (ISI).

In this paper, we evaluate hardware aspects of iterative receivers, and perform simulations assuming the transmitter described in Section I and the channel model presented in [9]. Two iterative receiver architectures are comparatively evaluated, detailed in the subsequent Section III.

The channel estimation block at the receiver implements the Time-Domain Least Square (TD-LS) estimation technique. The received $M \times 1$ symbol $\mathbf{Y}$ is written as

$$\mathbf{Y} = \mathbf{X}\mathbf{H} + \mathbf{W}, \tag{1}$$

where $\mathbf{X}$ is the diagonal $M \times M$ matrix of the training symbol, $\mathbf{H}$ is the $M \times 1$ Channel Frequency Response and $\mathbf{W}$ is the $M \times 1$ AWGN vector with variance N_0.

The LS estimate $\hat{\mathbf{H}}_{LS}$ of $\mathbf{H}$ minimizes the cost function

$$J(\hat{\mathbf{H}}) = \|\mathbf{Y} - \hat{\mathbf{H}}\|^2, \tag{2}$$

and it holds that

$$\hat{\mathbf{H}}_{LS} = \mathbf{X}^{-1}\mathbf{Y} = \mathbf{H} + \mathbf{X}^{-1}\mathbf{W}. \tag{3}$$

The LS channel estimate $\hat{\mathbf{H}}_{LS}$ for each subcarrier is

$$\hat{\mathbf{H}}_{LS}[k] = \frac{\mathbf{Y}[k]}{\mathbf{X}[k]}, \quad k = 0, 1, 2, \ldots, N-1. \tag{4}$$

The mean-square error (MSE) of the m-th subcarrier is

$$\sigma^2_{H_{LS},m} = \frac{\sigma^2_W}{\sigma^2_X} \tag{5}$$

which is inversely proportional to the SNR σ^2_X/σ^2_W. The comprehensive MSE is given by the sum of the MSE for every subcarrier and equals to the inverse SNR at the receiver:

$$\text{MSE}_{LS} = \sum_{m=1}^{M} \sigma^2_{H_{LS},m} = \frac{1}{\text{SNR}} \tag{6}$$

III. Receiver Architectures

In this section we propose a channel estimation technique that reduces the impact of erroneous decoded data at the iterative receiver. The error propagation affecting the channel estimation is minimized, resulting in higher performance than a conventional IEEE 802.11p receiver. In a conventional, non-iterative approach, the known pilot sequence at the receiver is used to compute the channel estimate from the transmitted pilot tones. In an iterative approach, the decoded bit stream $\mathbf{b_k}$ is used as a new training sequence.

In this work, a new channel estimation model is proposed. The model uses the weighted average of the channel coefficients computed by the known training sequence, and the iterative channel estimate coefficients computed by the decoded bit stream $\mathbf{b_k}$, treated as a new training sequence. It is described by

$$C_{\text{coeff}} = \alpha \times P_{\text{coeff}} + (1-\alpha) \times I_{\text{coeff}} \tag{7}$$

where C_{coeff} are the updated channel coefficients, α is a weight factor, and P_{coeff} are the channel coefficients computed by the known pilot tones and I_{coeff} are the channel coefficients computed by using the decoded bit stream to reconstruct the transmitted signal at the receiver and use it as reference for comparison resembling the use of the known pilot sequence.

Two hardware architectures are studied using this model. In the first architecture, namely A-I, the channel estimation which corresponds to the final decoded sequence is performed based on the channel coefficients computed from the previously processed OFDM symbol. In contrast, the second architecture, namely A-II, computes the channel coefficients from the same OFDM symbol.

The steps of one iteration of A-I are described in Algorithm 1, while the steps of one iteration of A-II are described in Algorithm 2. A visual representation of the proposed receiver for A-I is shown in Fig. 3, while a visual representation of the receiver for A-II is shown in Fig. 4.

IV. Simulation Results

The simulation parameters are summarized in Table II. A portion of the simulation results are presented in Fig. 5, 6. Fig. 5 presents the simulation results for BPSK modulation with code rate 1/2 in the V2V Expressway Oncoming scenario. Fig. 6 presents the simulation results for the same scenario for QPSK modulation with code rate 1/2.

In every scenario, in both BPSK and QPSK modulation schemes, both iterative receiver architectures outperform the

Algorithm 1 One Iteration of A-I

Step 1: The received k-th OFDM symbol $\mathbf{Y_k}$ is stored in a memory before it is equalized with the channel estimate $\mathbf{H_{k-1}}$ available at the time. If $k = 1$, the channel estimate is computed from the pilot tones, and stored for later use.
Step 2: The estimated 1st OFDM symbol, $\mathbf{X_k}$ is demapped, deiterleaved, decoded and descrambled.
Step 3: The decoded bit stream $\mathbf{b_k}$, is re-encoded, interleaved, scrambled and mapped, effectively creating a duplicate symbol $\mathbf{\tilde{A}_k}$. The decoded bit stream $\mathbf{b_k}$ is the final bit stream for the k-th OFDM symbol.
Step 4: The mapped sequence $\mathbf{\tilde{A}_k}$ is used as the pilot sequence for the stored symbol $\mathbf{Y_k}$, in order to perform the channel estimation task for the equalization of the $(k+1)$-th OFDM symbol, as described in (7). The stored pilot channel coefficients and the channel coefficients from the current channel estimate are used, resulting in a weighted average estimate $\mathbf{H_{k-1}}$. A new iteration begins.

Algorithm 2 One Iteration of A-II

Step 1: The received k-th OFDM symbol $\mathbf{Y_k}$ is stored in a memory before it is equalized with the channel estimate $\mathbf{H_{k-1}}$ available at the time. If $k = 1$, the channel estimate is computed from the pilot tones, and stored for later use.
Step 2: The estimated k-th OFDM symbol, $\mathbf{X_k}$ is demapped, deinterleaved, decoded and descrambled.
Step 3: The decoded bit stream $\mathbf{b_k}$, is re-encoded, interleaved, scrambled and mapped, effectively creating a duplicate symbol $\mathbf{\tilde{A}_k}$.
Step 4: The mapped sequence $\mathbf{\tilde{A}_k}$ is used as the pilot sequence for the stored symbol $\mathbf{Y_k}$, in order to perform the initial channel estimation task for the equalization of the k +1-th OFDM symbol, as described in Equation (7). The stored pilot channel coefficients and the channel coefficients from the current channel estimate are used, resulting in a weighted average estimate $\mathbf{H_k}$.
Step 5: The stored k-th OFDM symbol $\mathbf{Y_k}$, is equalized with the updated channel estimate $\mathbf{H_k}$ as described in equation 7, resulting in the updated OFDM symbol $\mathbf{X'_k}$.
Step 6: The updated OFDM symbol $\mathbf{X'_k}$ is demapped, deinterleaved, descrambled and decoded, achieving the final decoded bit sequence $\mathbf{b'_k}$.
Step 7: The received $(k+1)$-th OFDM symbol is equalized with the channel estimate $\mathbf{H_k}$, as described in step 1, and therefore a new iteration begins.

conventional, non-iterative receiver. In most cases, values of the parameter in the range α = 0.1–0.15 produce the best results, with a gain of 0.5 dB–1.5 dB in the region below the 10^{-1} BER area. The lower the BER percentage, the better our architectures perform, as the Viterbi decoder produces the correct decisions, therefore making the iteratively computed coefficients more effective. Comparing the architectures, there is no difference in performance between the two.

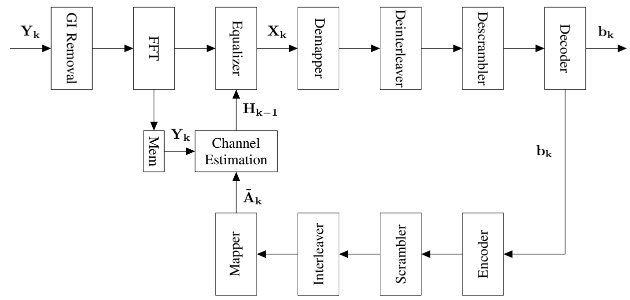

Fig. 3. Iterative Receiver for data aided channel estimation - A-I

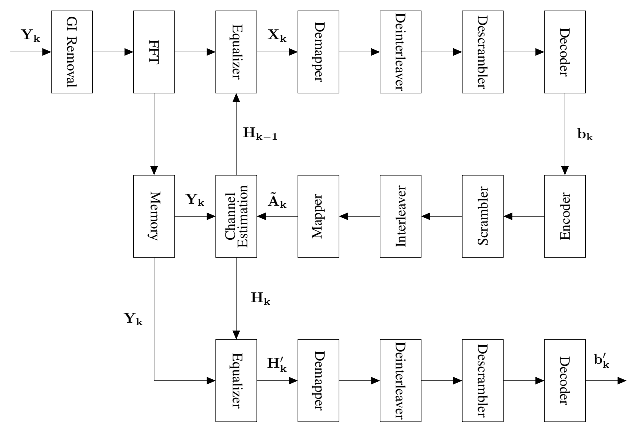

Fig. 4. Iterative Receiver for data aided channel estimation - A-II

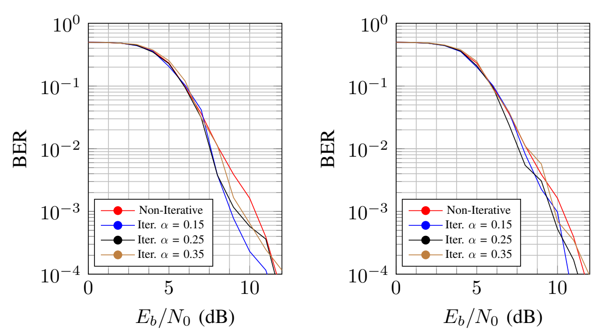

Fig. 5. Simulation Results for A-I (left) and A-II (right) architectures, BPSK Modulation, 1/2 Code Rate on V2V Expressway Oncoming

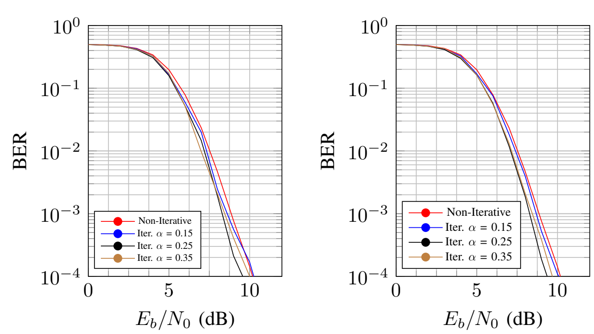

Fig. 6. Simulation Results for A-I (left) and A-II (right) architectures, QPSK Modulation, 1/2 Code Rate on V2V Expressway Oncoming

TABLE II
SIMULATION PARAMETERS

Parameter	Simulated Values
Centre Frequency	5.89 GHz
Bandwidth	10 MHz
Modulation Types	BPSK, QPSK, 16/64-QAM
Decoder Type	Viterbi
Packet Length	400 bytes
Simulated frames per E_b/N_0 value	200
α factor range	0.05 – 0.75
Channel Estimation	TD-LS with weighted average between the pilot and iterative coefficients
Channel Models	V2V, R2V Expressway and Urban Canyon

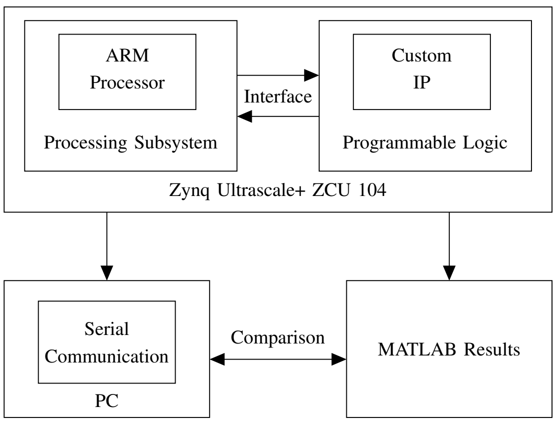

Fig. 7. Implementation and Verification Environment

V. HARDWARE ARCHITECTURE AND COMPLEXITY

A complexity comparison with the conventional IEEE 802.11p receiver of Fig. 2 has been made. The evaluated architectures were synthesized and verified on a Zynq UltraScale+ MPSoC ZCU104 Evaluation Board, using the Vivado and Vivado HLS synthesis tools. The implementation and verification environment is shown in Fig. 7.

Comparing the two architectures, an increase in the FPGA resources utilized in A-II -as expected- can be noticed. This increase -as stated- is not accompanied with improved performance results, despite executing a time-costly iteration in an attempt to improve the estimation of a particular symbol.

Comparing A-I, -the less complex architecture- with a conventional IEEE 802.11p receiver, there is a difference of 11% when it comes to BRAM utilization. There is also an increase of 407% regarding flip flops and an increase of 157% on the subject of Lookup Tables. However, the non-iterative receiver uses more DSP48s (11% increase). This is due to the fact that a conventional receiver has to deal with the whole frame at once, so more complex computations are needed. Table III details the utilized resources for each architecture.

Regarding the overall latency, the decoder block was the primary focus. While the FFT and IFFT blocks are the most demanding in terms of resources, the Viterbi decoder had the higher latency by a considerable amount (2000% in clock cycles more than any other block). Due to the many

TABLE III
UTILIZATION OF RESOURCES AND GAIN ACHIEVED

Receiver	BRAM	DSP48	FF	LUT	Gain (@10^{-3} BER region)
Non-Iter.	353	792	35960	69643	0 dB
Arch. A-I	397	705	182545	179109	1-2 dB
Arch. A-II	445	714	197452	201763	1-2 dB

dependencies, pipelining the block is a challenge. The latency is reduced by 400% using loop unrolling on the block with a factor of $K = 2$, but the utilized resources grow exponentially.

VI. CONCLUSIONS

In this paper, two alternative iterative receiver architectures for the time-varying vehicular channel have been studied and evaluated. The channel coefficients are computed by utilizing both the original pilot sequence and the decoded bit stream, instead of only the latter in previous works.

Two architectures have been presented. In the first architecture, the OFDM symbol processed in the previous iteration, contributes to the channel coefficients computation. In the second architecture, the contribution to the channel coefficients computation is made by the OFDM symbol processed at the time.

Simulations in four different V2V and V2I scenarios have been made. Both architectures outperform a conventional IEEE 802.11p receiver, but there is no difference in performance between the two, making the first architecture the more suitable one as it utilizes less hardware.

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