On-chip Power Line Communication for Cascaded H-bridge Power Converters

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***Abstract*— Distributed power generators and power converters are widely incorporated in modern microgrid and smart grid structures, which require data links among the source and load sites for monitoring and control. This paper proposes a novel power line communication (PLC) system design fabricated in an integrated circuit using the XFAB XH018 0.18μm CMOS technology to enable the data linking capabilities in such decentralized units. The proposed on-chip PLC system can be used in cascaded H-bridge power converters connected on a common DC or AC bus without requiring additional circuitry for transmitting the information. Also, its operation does not depend on the scale or type of the supplied load. An experimental prototype system for the power and data transmission, including the fabricated PLC chip and a field-programmable gate array (FPGA) device for the data reception, has been developed and tested. The experimental results verify the feasibility and effectiveness of the proposed on-chip PLC system.**

***Index Terms*— Power line communication, power converter, cascaded H-bridge, Smart Grid, Photovoltaic.**

I. Introduction

Energy systems based on spatially distributed power sources gradually gain popularity and commercial maturity, being deployed on automobiles [1], aircraft [2], the internet of things, up to the scale of smart cities and smart-grids [3-5]. One of the leading factors in this transformational landscape is the advent of new technologies on extended informatics that enable solutions towards the interlinking of the individual units in such networks. In principle, covering supervision and control requirements of essential or publicly exposed power systems suggests low tolerance of failure; thus, the respective network nodes need to establish secure connections with a central command point, to avoid compromising the exchange of vital information, proper synchronization, and data linking capabilities. For this reason, the power wiring is often utilized acting as the physical layer of communication to such links, implemented as power line communications (PLC) schemes.

The PLC technologies found in the literature can be classified into two main categories; those that use a separate coupling communication circuit and those that use the power converters to communicate through a common DC-bus. The studies of [6] and [7] use a coupling circuit connected in series or parallel with the power generating module in order to induce the respective information-driven excitation. This architecture's drawback is that modulation circuitry increases the overall power complexity and cost.

Another PLC architecture category that can reduce the aforementioned design implications is exploiting the power converter properties. This architecture has two subcategories, one where the power converters communicate through a common DC output bus and one where they communicate through a common DC input bus.

For the former subcategory, the exploitation focuses on some aspect of the power converter output characteristic that emerges as a result (or a sub-product) of its operating principle [8], [9]. The selection criterion of the modulation techniques found in the literature (PSK, SFM, BFSK, OOK, etc.) is usually the fitness to the nature of the emerging characteristic for exploitation. Although such approaches can yield interesting results, they all present application-specific solutions within a limited scope of realization.

For the latter subcategory, the focus is paid on manipulating some aspects of the power converters conventional operation by embedding the information signal into the driving control of the power switching unit of the converters (i.e., combining PSK/PWM, FSK/PWM, duty-cycle modulation, etc.) [10], [11]. Although equally interesting with the first subcategory, all these approaches are topology-limited as they need to exploit specific characteristics of the power converters.

Among the PLC techniques mentioned above, those based on power converters focus only on DC power solutions. Regarding the AC power implementations, studies of [12] and [13] investigate connecting the outputs of power converters in forms of series like H-bridges, AC-stacked inverters and relative topologies. However, neither has investigated the data transmission from the power units to a central remote data acquisition and/or control unit.

This paper proposes a novel PLC system design for cascaded H-bridge power converters, realized in an

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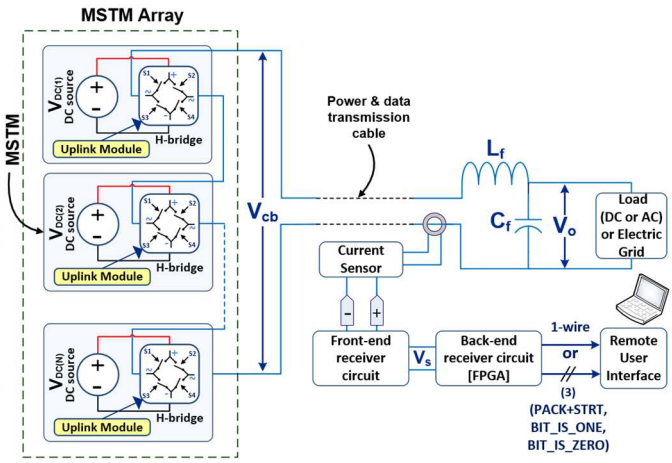


Fig. 1. Block diagram of the cascaded H-bridge structure under study with the proposed PLC scheme.

application-specific integrated circuit (ASIC), which enables the transmission of both power (DC or AC) and digital information through the same power line, avoiding the use of additional elements. This is achieved by exploiting the switch control driving pulses of the power modules output H-bridge. Compared to the techniques found in literature, the proposed design: *(i)* is employable in cascaded H-bridge modules for either DC or AC outputs, *(ii)* does not require additional modules in the power circuit for the transmission of information, and *(iii)* can be applied to a wide range of loads and scale. It is a flexible design that can be easily integrated into various solutions due to its versatility and scalability properties. The experiments verify the successful operation of the proposed ASIC unit and its ability to broadcast telemetry data.

The rest of this paper is organized as follows; Section II discusses the design of the proposed PLC transmitter implemented on-chip, and the off-chip receiver; Section III presents the simulation and experimental results, and finally Section IV concludes on the findings.

II. The Proposed Power Line Communication System

The main component of the PLC system under study is shown in Fig. 1 as a block diagram that shows an array of mixed (power and data) signal transmission modules (MSTMs) that supply either AC or DC power on a respective load. Each MSTM is based on a DC source of voltage $V_{DC,i}$ and a digital unit that controls the power switches of an H-bridge converter. This unit, indicated as 'Uplink Module' in Fig. 1, manages the switching patterns of the H-bridge to either produce a component of the voltage (which represents the overall power signal) or transmit data. The receiver acquires the information transmitted through the power cable by using a current sensor. The measured signal flows through a receiver comprised of an analog (front-end) and a digital (back-end) part, and finally, it is forwarded to a remote user interface (UI). A low-pass LC filter attenuates any high-frequency harmonics of the mixed power/data signal on the load side.

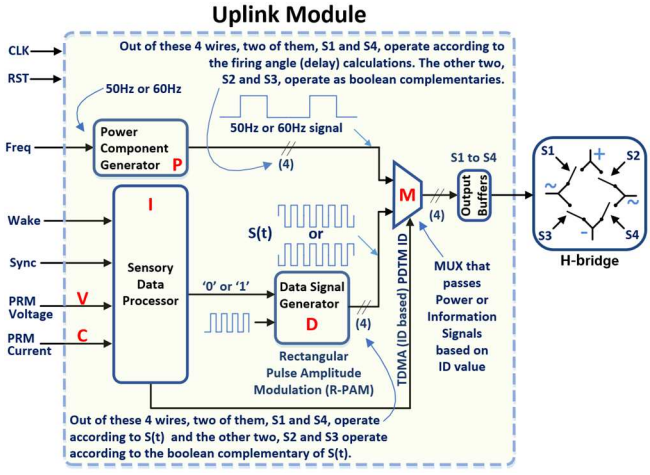


Fig. 2. Block diagram of the digital transmitter in each MSTM, that is implemented in an integrated circuit.

A. The proposed on-chip PLC digital data transmitter

The MSTM Uplink Module unit fabricated on-chip is depicted in Fig. 2. This unit undertakes the signal modulation acting as the transmitter interface of the system by creating suitable pulses for both streams (power and signal). In this work, the transmitter telemetry data consists of three bit-vectors (MSTM ID, DC input voltage, and DC input current). However, these parameters can be customized per target application. The ID bit vector is specified on every MSTM by an external digital hardwiring. As depicted in Fig. 2, the ID value covers two functions: *(i)* it instructs module 'P' for the expected width of the generated pulses (firing angle), and *(ii)* it defines the timeslot that the power signal output will be replaced by the data bitstream (using module 'M'). Block 'D' generates the information signal according to the serial information received by the block 'I'. The block 'I' includes an embedded cyclic redundancy check (CRC) polynomial [15] to embed a checksum at the end of the data packet. The transmitted symbols format follows the rectangular pulse-amplitude modulation (R-PAM), resembling the binary phase-shift keying (BPSK) technique. Block 'D' is based on a square-wave generator that negates the signal regarding the serial bits received by the 'I' block to create the 180° shift when needed. The vector sum of the digital signals created by the "P" blocks of each MSTM resembles a pseudo-sinusoidal voltage. In this work the MSTM array (Fig. 1) has been considered to form a cascaded H-bridge multilevel DC/AC inverter.

The measurements of the DC source voltage and current of each MSTM are input (i.e., 'V' and 'C' of Fig. 2) as 1-bit pulse-rate modulated (PRM) signals. The H-bridge becomes a short-circuit at a low-power state to allow for the current flow (i.e., power and data signals) of the rest MSTMs in series. When power is restored, the H-bridge keeps forming a short-circuit, waiting for a 'Wake' pulse. Each Uplink Module includes a PLL logic that can make the entire string self-calibrate and synchronize all power components of the pseudo-sinusoidal power signal. The 'Wake' signal operates similarly, but for the information synchronization, i.e., to dictate to each MSTM the right instance for transmission. Each MSTM employs a

built-in counter to calculate its dedicated timeslot based on its ID value. This counter's overflow triggers the "Sync" signal, which begins the data transmission. The user can access these signals for debugging and demonstration purposes, as shown in Fig. 2. The "CLK" input is connected to a clock signal. The "RST" input forces the uplink module to return to the initial state and sets the switches S1 to S4 to a halt, thus simulating a low-power event.

B. The proposed PLC receiver

The mixed power/data signal flowing through the power line is initially captured by a current sensor, as indicated in Fig. 1. Then, it is directed to the front-end part of the receiver for high-pass filtering and digitization. The output voltage, V_S, is forwarded to the back-end of the receiver, which is implemented on a field-programmable gate array (FPGA). This part implements a digital phase-locked loop and demodulator (PLL&D), which translates the received symbols into bits, and establishes a serial interface to forward the data packets (allowing for two connectivity options) to the remote UI. The block diagram of the receiver back-end is presented in Fig. 3. Block 'DF' removes any high-frequency spikes; the PLL ensures proper syncing with an internal square-signal generator (i.e. 'fc Gen' in Fig. 3), and an XNOR is used for the digital down-conversion (DDC) operation [16]. The blocks 'CNTR' and 'S/H' integrate and sample-and-hold the acquired digital data and forward them to 'SI', which creates two serial communication protocols. The '1-wire' adds a brief square wavelet-like oscillation at the start of every symbol using two different frequencies to mark the beginning of a packet or bit, respectively. These wavelets trigger the software frequency detectors to register this information appropriately. A simpler solution uses three separate wires (i.e. 'PACK+STRT', 'BIT_IS_ONE', and 'BIT_IS_ZERO') where a positive pulse, on any of these wires, signifies the receipt of a packet, a bit equal to '1' and a bit equal to '0', respectively.

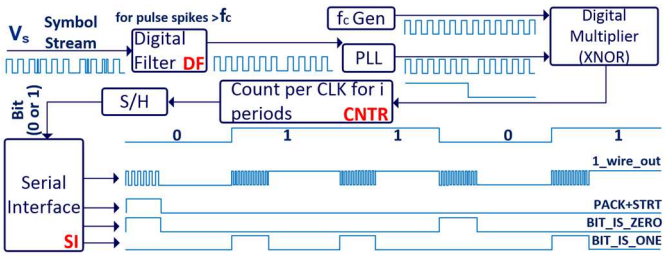


Fig. 3. Block diagram of the receiver back-end implemented on an FPGA.

TABLE I
SPECIFICATIONS OF THE EXPERIMENTAL PLC SYSTEM.

Parameter	Symbol	Value
MSTMs ID digital representation	R_1	10 bits
MSTM voltage resolution	R_2	10 bits
MSTM current resolution	R_3	10 bits
Sampling rate of MSTM array status	S	1 / min
Maximum number of MSTMs in the array	M	1000
CRC polynomial length	C	21 bits
Carrier frequency	f_c	40 kHz
Number of periods per binary symbol	i	22

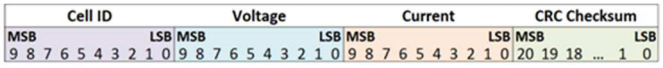


Fig. 4. Breakdown structure of the information in a data transmission packet.

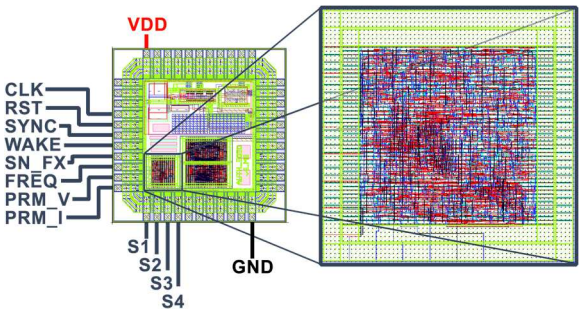


Fig. 5. The manufactured ASIC pinout and Uplink Module footprint.

C. Parameters selection in the proposed PLC system

In this study, a telemetry data packet was chosen to be the MSTM ID, sensed current, and sensed voltage; all represented as binary vectors holding R_1, R_2, and R_3 bits of resolution, respectively. The concatenated CRC checksum that is used for detecting transmission errors has C bits in length. So, one packet of information comprises $L = R_1 + R_2 + R_3 + C$ bits. The proposed PLC ASIC was designed according to the specifications presented in Table I. The breakdown of this structure and its serial representation, as it is broadcasted from the CRC checksum LSB to the Cell ID MSB is shown in Fig. 4.

III. SIMULATION AND EXPERIMENTAL RESULTS

The proposed PLC chip was designed by developing VHDL software code on Quartus Prime 18.1, while the VHDL coding was tested and simulated on ModelSim. The PLC chip synthesis was performed on the Cadence Virtuoso software suite. The back-end of the receiver was implemented on an FPGA development board based on an Altera chipset by Intel (10M50DAF484ES). The computer interface of an 8-channel Logic Analyzer was used for monitoring and capturing the PLC system I/O signals in real-time. Although the fabricated chip includes various additional features, the scope of this work solely focuses on the Uplink Module. Fig. 5 presents its pinout, footprint, and placement in the ASIC.

The simulation waveforms in Fig. 6 present the expected behavior of the outputs S1 to S4 when a falling-edge trigger pulse is applied on input 'Sync'. When a similar pulse is applied on 'RST', the system operates into the halt mode mentioned in § II.A. Once a negative-edge 'Wake' pulse is applied, the MSTM begins to control the H-bridge to create a square power component at 50 Hz or 60 Hz, according to the state of the 'Freq' input. The image capturing rendering of the S1 to S4 reveals the symbol phase-changes as extra thick- or light-colored stripes. Fig. 7 presents a test-bench of the Uplink VHDL code to be synthesized, certifying the unit's proper functioning. As designed, the 'Wake' pulses enable the H-bridge control circuitry and have no effect there-after other than resetting the internal timeslot estimator. The 'Sync' pulses trigger data transmission. For 'Freq'=1, the power component

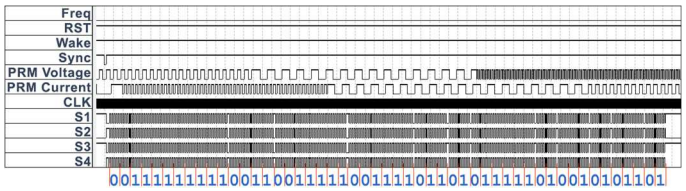


Fig. 6. Screenshot from Quartus testing that focuses on packet's phase changes.

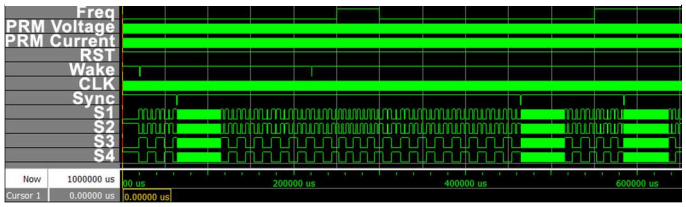
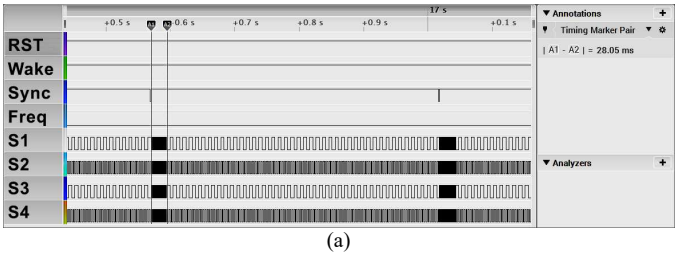


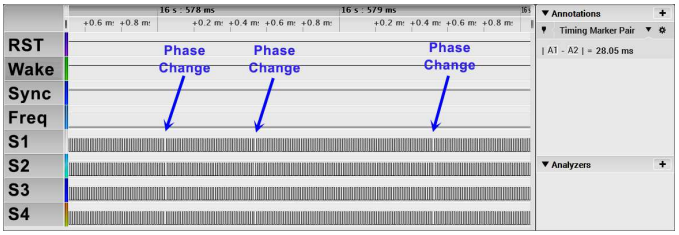
Fig. 7. Testbench screenshot from ModelSim.

frequency changes from 50 Hz to 60 Hz, proportionally narrowing the S1 to S4 square waves (Fig. 7).

The purpose of this study is to primarily verify the feasibility of the Uplink Module in a fabricated chip and the proper demodulation and serial communication of the receiver back-end as implemented on the FPGA board. For that purpose, one of the signals S1 to S4 is directly connected to the receiver's back-end input. The two pulse-rate modulated (PRM) sensory inputs of the MSTM are connected to two voltage-controlled oscillators (VCOs) to simulate the generation of voltage and current measurements. The 'CLK' is supplied by an external generator, and the 'RST', 'Freq', 'Wake', 'Sync' inputs are controlled by an Arduino-based microcontroller board, which provides valuable low-frequency user feedback for debugging and demonstration purposes. Each symbol was divided into 22 periods of 25 μsec each. The symbol duration is 22 x 25 = 550 μsec, and the baud rate is 1818.2 bps. Since a data packet includes 51 bits of information, the packet duration is 51 x 550 = 28.05 msec.



(a)



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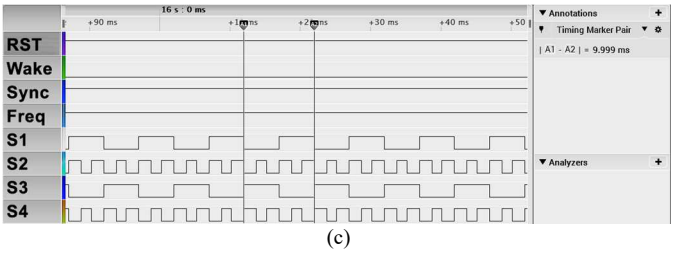
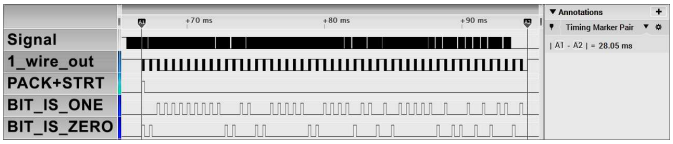
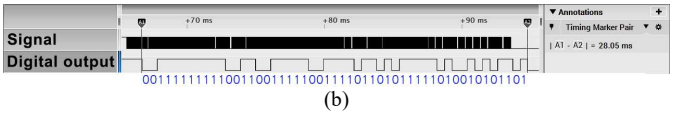


(c)

Fig. 8. Logic analyzer experimental waveforms: (a) transmission of two 51-bit data packets, triggered by a 'Sync' falling-edge event, (b) five symbols that correspond to bits '01001', (c) transmission of H-bridge driving signals to produce a component of the power signal of 50Hz with 60° degrees firing angle.



(a)



(b)

Fig. 9. (a) Logic analyzer experimental waveforms that reveal an enlarged part of the signals that the digital logic of the proposed PLC receiver is demodulating, (b) the demodulated bitstream.

Enlarged parts of the four H-Bridge driving signals (S1 to S4) are shown in the experimental waveforms depicted in Fig. 8. In Fig. 8(a), the falling event of the 'Sync' signal triggers twice the transmission of the MSTM telemetry data. The signals 'RST' and 'Wake' are fixed to logic 1, suggesting a disable state for both. The timing markers show that the packet to be transmitted requires approximately 28.05 msec. Fig. 8(b) presents a zoomed snapshot of the area focused on the phase change of the information signal. The waveforms start by a '0' bit followed by a '1' bit, followed by two '0' bits, followed by a '1' bit, transmitting the symbols corresponding to the bit sequence '01001' i.e., the bits 40 to 44, also shown in Fig. 6. Fig. 8(c) reveals the bridge driving signals that produce the ID-specific power component in detail.

Fig. 9(a) depicts the logic analyzer experimental waveform of the bitstream that has been sent by the uplink transmitter (indicated as 'Signal') against the received data by the remote UI. The acquired bitstream 'Digital Output', shown in Fig. 9(b), changes logic states in the same order as the symbols shown in Fig. 6, simulated for the same VCO frequencies. Also, three extra experiments were conducted verifying that, for the given 21-bit CRC polynomial (i.e. 101100101011101010001) that is embedded in the fabricated ASIC, the received 20 last bits (checksum) have been identical to the anticipated ones, in all cases. Three indicative cases are the following; (a) a preset (fixed) 30-bit vector that bypasses the chip measurements and sends a fixed vector instead (this is done by raising the 'SN_FX' pin shown in Fig. 5, to logic '1'):

Fixed Value: 00111 11111 01010 10101 00001 11101
CRC checksum: ***11110000011111000111***

(b) when both sensors are sensing no pulses:

Sensing Zero: 11111 00000 00000 00000 00000 00000
CRC checksum: ***11101000000011100110***

and (c) for a random sensing value:

Sensing Random: 11111 00000 01000 00101 11100 00111
CRC checksum: ***00000111010110000000***

The result of the comparison between the bitstreams of Fig. 6

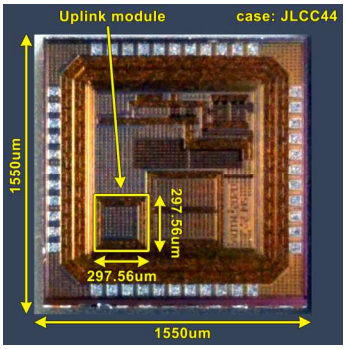


Fig. 10. Microscope photograph of the manufactured ASIC with the dimensions of the chipset and the Uplink Module placement.

and Fig. 9(b) and the three verified CRC checksums confirm that the data have been successfully received and that the Uplink Module operates as intended. A microphotograph of the manufactured chip in a JLCC44 case is shown in Fig. 10. Its power consumption is 172.5 μW (V_{dd}=2.3 V, I_{vdd}=75 μA) when the chip is clocked at 2.0 MHz.

IV. Conclusion

Among the available PLC implementation solutions, the most advantageous alternatives in terms of cost and simplicity are the ones that do not require additional components in the power circuit. This paper analyzes the on-chip implementation of a novel method that exploits the H-bridge control signals in cascaded H-bridge power converters to transmit both power and digital data. Compared to the solutions found in the literature, the proposed design can be applied in cascaded H-bridge converters with either AC or DC output needs no additional power amplifier or coupling circuit for data transmission, and can be applied on any scale and any power-supplied load. It offers a communication enabling technology to stacked power converters (e.g. [13], [14]) if controlled power switches are appropriately integrated at their output. Hence it is scalable, highly versatile, and presents low implementation complexity.

The proposed PLC technique was implemented in an ASIC using the XFAB XH018 0.18μm CMOS technology. The simulation and experimental results presented in the paper verified the successful operation of the fabricated PLC chip.

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