BTI Aging Influence on Charge Pump Circuits

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***Abstract* – Charge pumps are widely used in modern nanometer technology circuits. Due to the high voltage levels that are generated in the internal nodes of these circuits, the influence of bias temperature instability (BTI) phenomena on their aging is expected to be substantial. In this paper we study the BTI related aging of various charge pump circuits and aging related simulation comparisons are presented.**

Index Terms – Charge pump circuits, BTI influence, Aging.

I. Introduction

Bias Temperature Instability (BTI) is a crucial reliability issue since it degrades the performance of p- and n- channel MOSFETs used in CMOS circuits. BTI results in a gradual shift in MOSFET characteristics, such as threshold voltage (V_{th}), transconductance (g_m), subthreshold slope (S), linear and saturation drain current (I_{DLIN} and I_{DSAT}), etc., over time, and hence in-turn degrades the performance of digital memory and analog CMOS circuits. As a result, the operating lifetime of CMOS devices and circuits is reduced, and if it is not detected, BTI can lead to premature failure of Integrated Circuits (IC) chips. BTI degradation of p-MOSFET (pMOS) devices is known as Negative Bias Temperature Instability (NBTI). On the other hand, BTI degradation of n-MOSFET (nMOS) devices is known as Positive Bias Temperature Instability (PBTI) [1].

A charge pump (CP) circuit is a DC-DC converter for the generation of various voltage levels from a power supply voltage. It is commonly used as a voltage generator in various applications as part of an IC, like in Flash memories, DRAMs, power electronics e.t.c.

In this paper we present a study on the influence of BTI aging on various CP circuits in the literature. In Section II preliminaries are presented on BTI and the BTI influence model as well as on the CP circuits under consideration. In Section III, the simulation results and comparisons are presented while in Section IV the conclusions are drawn.

II. Preliminaries

A. Bias Temperature Instability

There are two categorizations of BTI: Static BTI in which the transistor is under constant stress (high gate bias and temperature) without recovery, and Dynamic BTI in which the transistor alternatively undergoes the stress and recovery phases. For both cases, the BTI effect is modeled as a threshold voltage shift (ΔV_{th}) [2].

In our simulations, we used the Dynamic BTI model equations according to [2], since a CP is in a continuous mode of operation under the control of a clock signal. These equations are presented below, while all the parameters are presented in Table 1.

$$\Delta V_{th}^{dynamic} = \left(\frac{\sqrt{K_v^2 \alpha T_{clk}}}{1 - \beta_t^{1/2n}} \right)^{2n} \tag{1}$$

$$\beta_t = 1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C (1-\alpha) T_{clk}}}{2t_{ox} + \sqrt{Ct}} \tag{2}$$

TABLE I
Parameters of Dynamic BTI Equations

K_v	$\left(\frac{qt_{ox}}{\epsilon_{ox}}\right)^3 K^2 C_{ox}(V_{GS} - V_{th})\sqrt{C}\exp\left(\frac{2E_{ox}}{E_0}\right)$	
E_{ox}	$\frac{V_{GS} - V_{th}}{t_{ox}}$	
C	$T_o^{-1} \cdot exp(-E_a/kT)$	
t_e	if $t - t_0 > t_1$	t_{ox}
	otherwise	$t_{ox}\sqrt{\frac{t - t_0}{t_1}} - \sqrt{\frac{\xi_2 C(t - t_0)}{2\xi_1}}$
t_0	time at which stress phase begins	
t_1	time at which recovery phase begins	
$E_a(eV)$	0.49	
$E_0(V/nm)$	0.335	
δ	0.5	
$K(s^{-0.25} \cdot C^{-0.5} \cdot nm^{-2})$	8×10^4	
ξ_1	0.9	
ξ_2	0.5	
T_o	10^{-8}	

In order to model the BTI impact on the transistors, we used a DC voltage source at the gate of every transistor as shown in Fig. 1 [4].

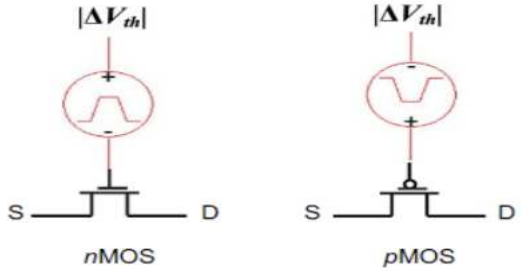


Fig. 1. BTI modeling in nMOS and pMOS devices.

B. The Charge Pumps under Consideration

In this work, we studied the influence of the BTI phenomenon in five charge pump circuits. In each case, we consider a two stage charge pump topology. Next these topologies are presented:

1) *Dickson CP with pMOS [5]*: The topology is presented in Fig. 2. Among the advantages of this charge pump are the efficient voltage boosting and current drivability irrespectively of pump stages, even with fairly high parasitic capacitance values (C_{PAR}). Dickson's charge pumps are applicable in non-volatile memories albeit deficiencies in low voltage cases below 2V. This drawback is due to V_{th} drops when MOS's body terminals are reverse-biased resulting in reduced charge transfer to later stages. The body effect increases with the stages and reduces gain. In addition, low voltage operation reduces charge pump's effectiveness in turning on MOS diodes due to threshold limits and conventional body biasing [3].

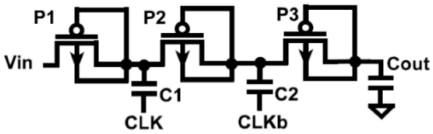


Fig. 2. Two stage Dickson charge pump.

2) *Two-Branch Dickson CP [6]*: The dual-branch structures were introduced to lower ripples in the Charge Transfer Switches (CTS) design and later evolved into latch-based designs. This topology (Fig. 3) offers smaller C_{PUMP} values and half the output ripple (V_R) compared to single branch CPs. The aforementioned advantages translate to voltage drop (V_{DROP}) reduction, higher switching frequencies and the possibility of low voltage (LV) start-up. Although, ripples associated to noise that affects loads such as memory can be reduced by increasing C_{OUT} and f_{CLK}, these strategies adversely lengthen ramp-up time and reduces pump efficiency respectively. Nevertheless dual-Branch CPs are not suited for LV operation and cold-start circuits [3].

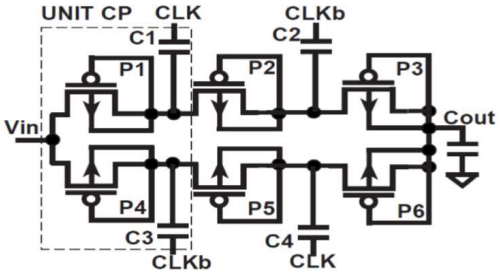


Fig. 3. Two-Branch Dickson charge pump.

3) *Series-Parallel CP [7]*: In this topology (Fig. 4), efficient control of gate voltages can reduce percentage V_{th} drops in MOS devices. The major drawback of this CP includes the C_{PAR} associated with the three extra switches per stage which affects performance and the V_{OUT} which strongly decreases with stage number [3].

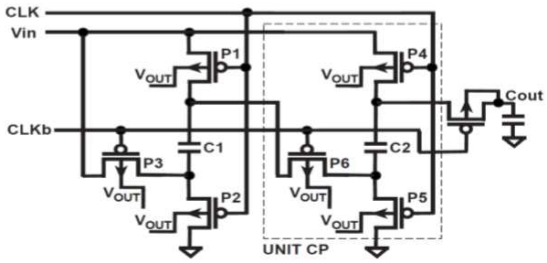


Fig. 4. Series-Parallel charge pump.

4) *Latch Based CP [8]*: This topology (Fig. 5) improves pumping efficiency and reduces ripples, and also enhances charge transferability while requires smaller capacitances (half the original C_{PUMP} size), which in turn reduces the effect of devices sizes on V_{th}. Moreover, redistribution loss is also reduced as the branches complements charge transfer to the output node, ensuring load voltage stability. Latch Based CP has intertwining anti-phase clock signals on two branches with source-connected nMOS bulks to eliminate body effect. This structure with two latch-based branches eliminate V_{th} drops for an almost full charge transfer between stages, but it is still not suited for LV applications [3].

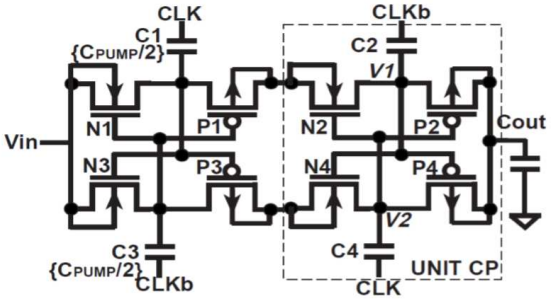


Fig. 5. Latch based charge pump.

5) *Exponential Gain CP [9]*: Exponential CPs (Fig. 6) have voltage gain exponentially associated to their pumping stages. This structure proposed to reduce charge pump stages with the same achievable gain, considering per-stage V_{th} drop in MOS switches. The Exponential Gain CP also suppresses V_{th} problems by having a larger clock voltage growth rate as compared to V_{th} drop rate. This solves the voltage saturation issue due to augmented V_{th} and lower V_{OUT} in linear structures [3].

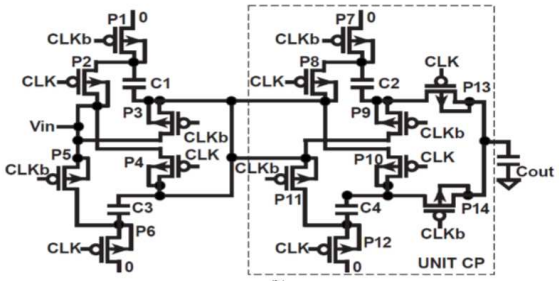


Fig. 6. Exponential Gain charge pump.

III. Simulation Results

All five CPs have been designed in the 90nm CMOS technology of UMC (nominal V_{DD}=1V) using the Virtuozo platform of CADENCE along with the SPECTRE simulator. In all CP designs, the input voltage was V_{in}=1V, the internal capacitances was C_{PUMP}=10pF, the output load (a parallel connected pair of a capacitor and a resistor) was equal to C_{OUT}=500pF and R_{OUT}=50KΩ, while all transistor sizes were W/L=3μm/80nm. In order to estimate the threshold voltage shift of every transistor in a CP, we initially measured, under BTI free conditions, the maximum gate-source voltage (V_{gs}), as well as its duty cycle (α) for every transistor. Afterwards, using (1), we calculated ΔV_{th} for every transistor, for time periods of 1, 3, 5, and 8 years. Finally, running the simulation for every CP, under BTI influence we measured the max output voltage level (V_{OUT}) and the ramp-up time (t_{ru}), which is the time required to reach 90% of V_{OUT} at the CP output.

Aiming to calculate ΔV_{th} for the first year we used the initial V_{gs} without stress. For the third year we calculated ΔV_{th} using V_{gs} from the second year etc. However, the differences in the V_{gs} of the transistors between the years were negligible. Some transistors in Series-Parallel, Latch Based and Exponential Gain Structure CPs had V_{gs} > 1V, which shows that these transistors are highly affected from BTI due to the increased bias stress. Tables 1 and 2 show the change in V_{OUT} and t_{ru} for each one of the aforementioned CPs, without stress (fresh) and after 8 years of BTI stress, in 27°C and 85°C respectively.

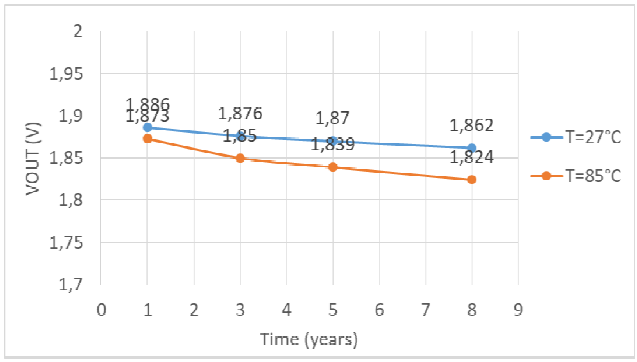
TABLE 1
BTI Influence on V_{OUT} and t_{RU} in 27 °C

	V_{OUT} (V)			t_{ru} (μs)		
CP	Fresh	8y Aged	%	Fresh	8y Aged	%
Dickson	1.918	1.862	-2.9	4.44	4.52	1.8
2-Branch Dickson	1.179	1.154	-2.1	4.43	4.48	1.1
Series-Parallel	1.368	1.43	4.5	3.09	3.87	25.2
Latch Based	2.917	2.914	-0.1	1.67	1.87	11.9
Exponential Gain	1.382	1.457	5.4	2.76	3.63	31.5

TABLE 2
BTI Influence on V_{OUT} and t_{RU} in 85 °C

	V_{OUT} (V)			t_{ru} (μs)		
CP	Fresh	8y Aged	%	Fresh	8y Aged	%
Dickson	1.939	1.824	-5.9	4.51	4.67	3.50
2-Branch Dickson	1.222	1.175	-3.8	4.75	4.91	3.36
Series-Parallel	1.354	1.469	8.5	3.02	5.04	66.00
Latch Based	2.911	2.900	-0.4	1.75	2.28	30.20
Exponential Gain	1.370	1.517	10.0	2.60	4.86	86.90

Next, the simulation results are presented for each CP (Dickson in Fig. 7, Two-branch Dickson in Fig.8, Series-Parallel in Fig. 9, Latch Based in Fig. 10 and Exponential Gain in Fig. 11) that accentuate the influence of BTI on V_{OUT} and t_{ru} across the years, for the temperatures of 27°C and 85°C. Note that either an increase or decrease of the V_{OUT} should be considered as a specification violation.



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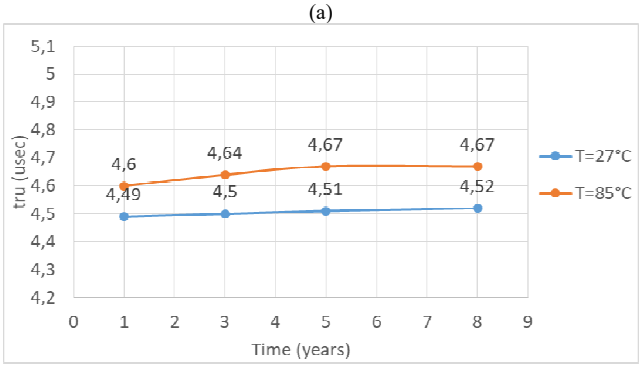

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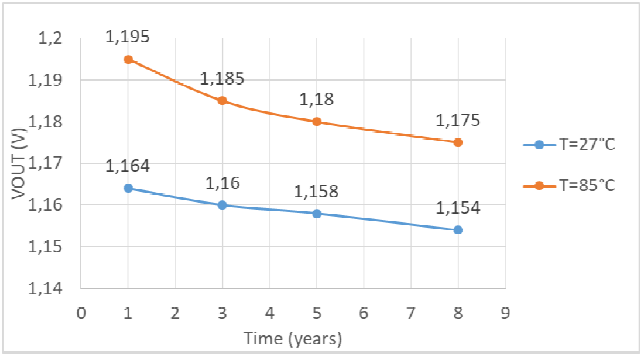
Fig. 7. Dickson CP: a) V_{OUT} and b) t_{ru} as a function of time.



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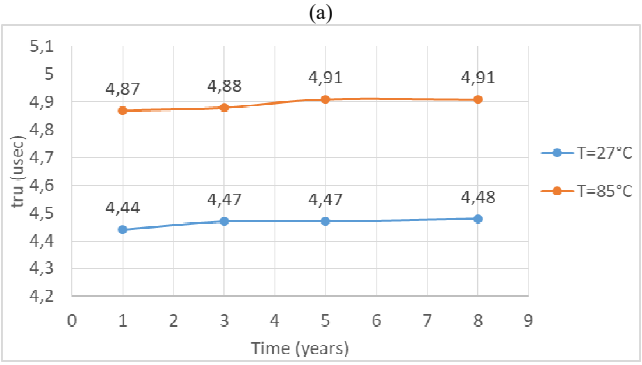

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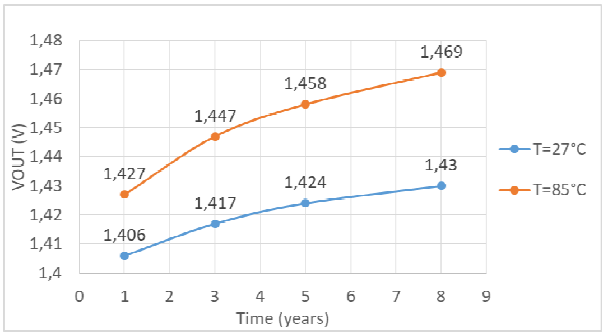
Fig. 8. Two-branch Dickson CP: a) V_{OUT} and b) t_{ru} as a function of time.



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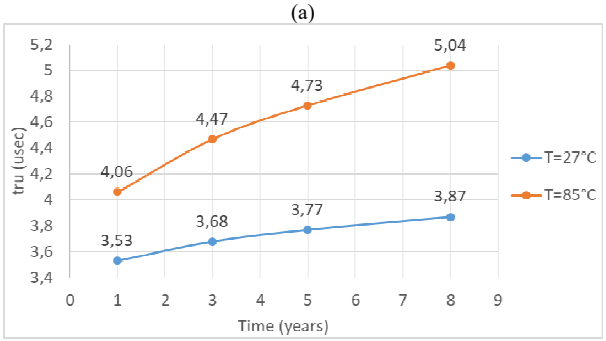

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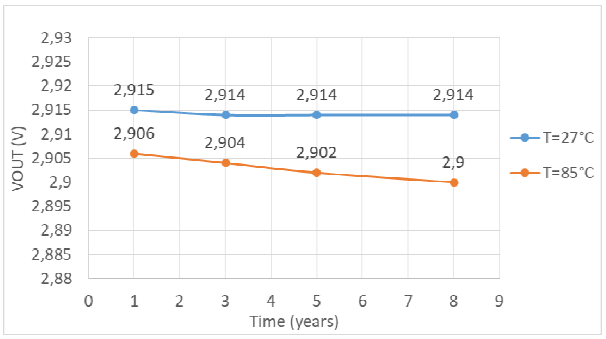
Fig. 9. Series-Parallel CP: a) V_{OUT} and b) t_{ru} as a function of time.



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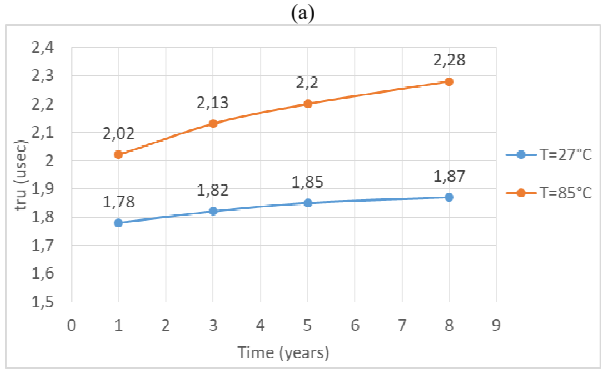
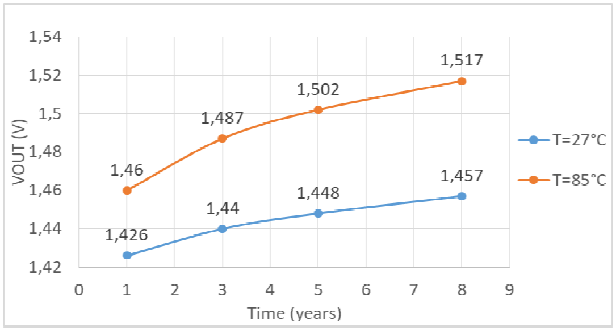


(b)

Fig. 10. Latch based CP: a) V_{OUT} and b) t_{ru} as a function of time.

IV. Conclusions

A study on the BTI related aging of five charge pump circuits is presented in this paper. Simulation results indicate the influence of BTI on the CP generated output voltage (V_{OUT}) and ramp-up time (t_{ru}). The Dickson and the Two Branch Dickson topologies showed a small decrease in V_{OUT} over the years, in both 27°C and 85°C. In addition, there was a small increase in t_{ru}. The voltage stress is lower in these CPs and thus they are slightly affected by transistor BTI. The Latch Based topology presents a negligible decrease on V_{OUT} but a significant increase on the t_{ru}. On the other hand, the Series-Parallel and Exponential Gain topologies show an increase in their V_{OUT} over the years and a substantial increase in the t_{ru} with the aging of their transistors, where t_{ru} increases 66.0% and 86.9% respectively, at the temperature of 85°C.



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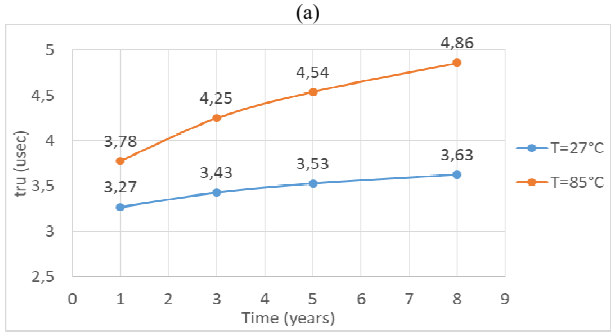

(b)

Fig. 11. Exponential Gain CP: a) V_{OUT} and b) t_{ru} as a function of time.

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