# Compact Ground Bounce Sensors for SoC Energy Harvesting Applications

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*Abstract*— **In this work, the energy harvesting system on chip ground bounce monitoring is addressed, by designing and comparing three ground bounce sensors. Special focus is given in compact sensors implementations, and in particular in the bulk driven MOSFET sensor, in the source follower – transconductor (SF+Gm) and in the DC coupled one. The sensors gain-bandwidth performance trade-off is addressed and all three are designed in an RFCMOS process. Their performance is demonstrated by advanced simulations results, taking into account temperature and process variations, and providing all related metrics from gain/bandwidth to linearity, power consumption and silicon active area. Selection criteria are extracted since each of these sensors is optimum to be used in different applications versus specific performance metrics.**

*Keywords—ground bounce, integrated sensors, on the fly converters supply monitoring*

## I. INTRODUCTION

Ground bounce is the amount that a ground return rises or falls relative to the system's 0V reference, and, in a DC-DC switching converter, ground bounce can have large amplitude, often because of changing magnetic flux. Therefore, especially in energy harvesting applications supply monitoring is a really crucial task. DC-DC converters, and buck and boost circuits in general, pound the ground with fast-changing currents. When the supply nodes are not stable, system performance suffers and EMI issues occur. An accurate monitoring and optimization of ground bounce is needed, as to enable an intuitive sense for reducing or optimizing the problem [1]-[3]. Low magnitude voltages have to be sensed and amplified, over a very wide bandwidth. In complex System on Chip (SoC) applications, the requirements of a compact supply sensing circuit, being capable of measuring very low amplitude signals from DC up to GHz and beyond, without contaminating the measurement, have to be met [1]-[3].

Specifically, particular requirements must be satisfied [4]-[5] as to enable ground bounce monitoring without spending active chip area. The sensor must not affect the noise propagation, since it is not part of the SoC function. In addition, the signal must not be contaminated from interconnect crosstalk, which is important in complex SoC chips, where noise from surrounding circuits can couple to the interconnects. The monitored bandwidth must extend down to DC and high enough to be able to measure all the intermodulation products while providing adequate gain. In SoC applications, the bandwidth (*BW*) in focus is in GHz as to achieve an accurate on the fly measurement. Wideband techniques in the design are essential to achieve the high frequency response but without using area-consuming structures. The sensing topology needs to be compact and occupy as less area as possible, for practical implementation in SoC applications, where the area to cost ratio is one of the product driving factors. Finally, while the gain is not a tough specification, since high performance spectrum analyzers can measure signals down to approximately -170 dBm, the gain - bandwidth performance should be accessed, since the sensor acts as buffer between the supply taps and the 50Ω load of the spectrum analyzer *(SA)* and prevents shunting the substrate to ground that would affect noise propagation [4]-[5].

In this work three compact power supply monitoring sensors are addressed. They are designed and simulated in a 65 *nm* RFCMOS process. They are optimized for gain bandwidth performance and they are benchmarked versus their efficiency to be used for SoC energy harvesting applications.

## II. SUPPLY MONITORING IC SENSOR DESIGNS

Three compact ground bounce sensing topologies are designed and assessed. Bulk driven MOSFETs, the source follower – trans-conductor (SF+Gm) sensor [4] and the DC-coupled PMOS Sensor [5].

### A. Bulk Driven MOSFET Supply Sensing

The dominant mechanism of ground noise injection in MOS devices is the body effect. In contrast to noise coupling through the source and drain depletion capacitances, which becomes more pronounced in high frequencies, the body effect is also important in the low frequency region. NMOS transistors fabricated on the p-substrate can be used to sense supply ground noise via the drain current modulation due to the source-body trans-conductance $g_{mb}$. The sensing technique is depicted in Fig.1.
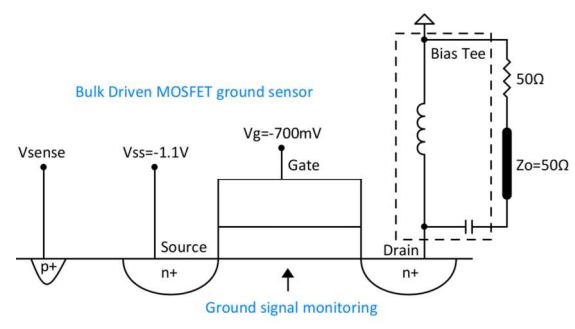


Fig. 1.    Bulk Driven MOSFET sensors

An NMOS transistor is connected to the spectrum analyzer 50Ω input through a bias tee which is used to set the DC bias point independently of the AC signal. The inductor high

impedance does not allow the *AC* signal to flow through it, but at *DC* it is a short-circuit and sets the bias point of the drain to 0 V. The capacitor provides a low impedance path for the *AC* signal to the spectrum analyzer input. Since the input is connected to ground, typically the NMOS has to be biased from negative power supplies. This is easy in simple test chips but impractical is production environments. The gain is proportional to $g_{mb}$ which is given by,

$$g_{mb} = \frac{\gamma g_m}{2\sqrt{V_{SB} + |2\Phi_F|}} \qquad (1)$$

where $g_m$ is the transistor transconductance, $\Phi_F$ is the fermi potential $\gamma$ is the body-effect constant. Therefore, the gain mainly depends on the bias current and the transistor dimensions, as provided in equation 2.

$$G = g_{mb}Z_o \approx g_m Z_o \approx Z_o \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \qquad (2)$$

$Z_o$ is the load resistance at the drain node (50Ω), $\mu_n$ is the electron mobility, $C_{ox}$ is the gate oxide capacitance, $I_D$ is the drain current, $W$ is the width and $L$ is the length of the transistor.

### B. Source Follower – Transconductor (SF+Gm) Sensor

The *SF+Gm* sensor is provided in Figure 2 [4]. The circuit is composed of a source follower (*M1-M2*), a transconductance stage (*M3*) and a current mirror stage with current amplification (*M4, M5*). A bias tee is used in the output.
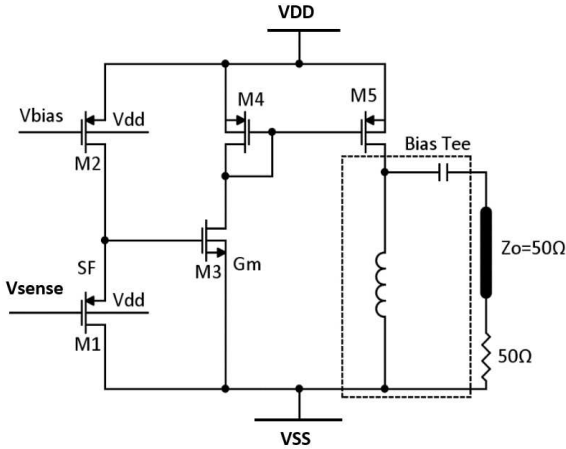


Fig. 2.    Source Follower – Trans-conductor (SF+Gm) Sensor Schematic

The sensed voltage signal at the input of the source follower is level-shifted and driven to the gate of *M3*. This voltage is translated to a drain current $I_{D-M3}$ and mirrored by *M4-M5* to the output. The gain is given by the following equation.

$$G = A_{vSF} g_{m3} \frac{\left(\frac{W}{L}\right)_{M5}}{\left(\frac{W}{L}\right)_{M4}} Z_o \qquad (3)$$

$A_{vSF}$ is source follower gain, which is equal to

$$A_{vSF} = \frac{g_{m1}}{g_{m1}+G_{s1}} \qquad (4)$$

where $G_{s1}$ is the total conductance at the source of M1, including the body-effect transconductance $g_{mb}$.

### C. DC-Coupled PMOS Supply Sensor

The sensor schematic is provided in Fig. 3 [5]. This measurement technique uses PMOS-based differential sensors DC coupled to the substrate/supply taps. Since no input capacitor is used, the measurement bandwidth can expand down to DC. The main advantage of this method, over the previous, is that the sensor measures the signal in differential mode. The differential-to-single action of the balun at the output, removes the common mode noise of the ground and the signal coming from the substrate. Therefore the signal integrity from the measurement point to the input of the measurement instrumentation is preserved. In physical circuit layouts containing NMOS and PMOS transistors, substrate shunting contacts are often used to prevent latch-up. A careful layout reduces this problem, but a circuit with only PMOS transistors as the sensor mentioned here ensures no interaction with the substrate noise propagation. The output can be connected to SA (off-chip) or an on-chip digitizer. In the first case, buffers must be used in the output to match the sensor's output resistance with the 50Ω impedance of the SA. Because the output common mode DC voltage is in the input range of analog multiplexers, the sensor output can be easily multiplexed.
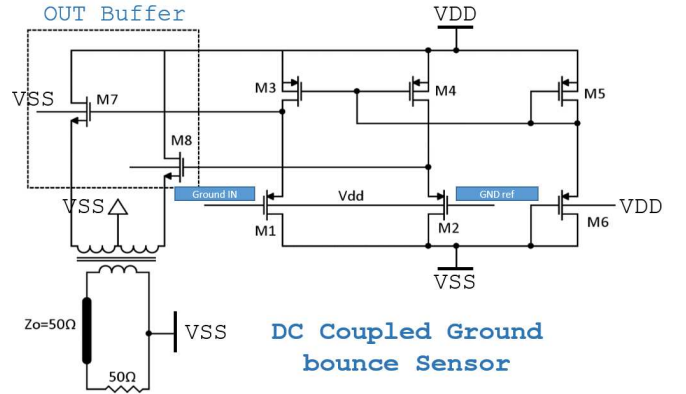


Fig. 3.    DC-Coupled PMOS ground sensor schematic

The sensor circuit consists of two transistors branches of *M1, M3* and *M2, M4*. Transistors *M5* and *M6* are used to provide a self-generated bias. Variations of the bias current caused by power supply ($V_{DD}$) fluctuations are suppressed as common mode *AC* signal due symmetry. *M7* and *M8* are NMOS source followers used as buffers to match the sensor output impedance to the transmission line.

The gain can be evaluated with the help of the small signal model of the sensor without the buffers which is depicted in Fig. 4 [5].
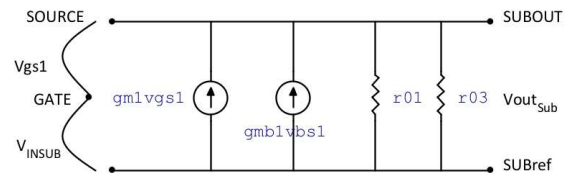


Fig. 4.    Small signal model of the DC-Coupled PMOS sensor [iorga]

$V_{OUTSUB}$ is the sensor differential output, and $V_{INSUB}$ is the input sensed substrate/supply signal. The SUBREF node is considered a virtual ground in this analysis because it does not vary with the substrate input voltage $V_{INSUB}$. The output voltage can be expressed by the equation:

$$V_{OUTSUB} = V_{INSUB} \frac{g_{m1}(r_{o1}||r_{o3})}{1 + (g_{m1} + g_{mb1})(r_{o1}||r_{o3})} \qquad (5)$$

If $(g_{m1} + g_{mb1})(r_{o1}||r_{o3}) >> 1$, which is usually the case, the amplifier gain becomes equal to

$$\frac{V_{OUTSUB}}{V_{INSUB}} = \frac{g_{m1}}{g_{m1}+g_{mb1}} \qquad (6)$$

Buffer transistors *M7* and *M8* were scaled for output resistance of about 50 Ω, to match the transmission line impedance and avoid oscillations and reflections. The buffer output resistance, forms a resistive divider with the transmission line $Z_o$. Therefore, the total gain is equal to,

$$G = \frac{g_{m1}}{g_{m1}+g_{mb1}} \frac{Z_o}{R_o+Z_o} \cong \frac{1}{2} \qquad (7)$$

where $R_o$ is the buffer output resistance.

### III. SIMULATION RESULTS AND BENCHMARKING

The above three ground bounce sensors are analyzed and simulated in 65 *n*m *RFCMOS* process, using Cadence Virtuoso suite and the Spectre/RF simulator. The supply voltage was set to 1.1V. Since a sub-micron technology node is used, small channel effects such as Channel Length Modulation (CLM) and Drain Induced Barrier Lowering (DIBL) are expected to have a strong influence.

The respective transistor sizing of the sensors is given in Table 1.

TABLE I.    SENSORS TRANSISTOR SIZING

| Supply Bounce Monitoring Sensors | | | |
|---|---|---|---|
| MOSFET | Bulk Driven MOSFET | SF-gm Follower | DC coupled PMOS Sensor |
| | (W/L) sizing in $\mu m$ | | |
| M1 | 190/0.09 | 48/0.12 | 48/0.12 |
| M2 | n.a. | 48/0.12 | 20/0.12 |
| M3 | n.a. | 16/0.12 | 48/0.12 |
| M4 | n.a. | 12/0.12 | 20/0.12 |
| M5 | n.a. | 50/0.12 | 2/0.06 |
| M6 | n.a. | n.a. | 6/0.06 |

All sensors were optimized as to provide the best gain – *BW* performance, meaning that the *BW* performance was stretched to the maximum feasible value while keeping a reasonable gain.

In relation to the bulk driven sensor, depicted in Fig. 1, the simulated values of the gate-source and body-source transconductance are $g_m$=100 mS and $g_{mb}$=16.1 mS yielding a ratio of $g_{mb}/g_m = 0.161$. Since high-frequency behavior is addressed, the s-parameter simulation of the sensor performance (gain / bandwidth) for process and temperature variations, is provided in Fig. 5(a).

Although the *BW* extends down to *DC* and is relatively high, the sensor accuracy is limited by its low gain as a result of the small source-body transonductance $g_{mb}$. If a higher gain is required, the bias current can be further increased. However, the power consumption may become too high. Additionally, a high biasing current requires wider metal interconnects that result in higher parasitic capacitances values. Apart from the low gain, the main disadvantage of the bulk-driven sensor is its single-ended output that is susceptible to interconnect and ground bounce crosstalk. Additionally, dedicated pins are required for each transistor and the outputs cannot be multiplexed. Therefore, its applications are limited to experimental test designs.

The gain of the *SF+Gm* sensor can be easily calculated by substitution of the simulated transistor operating points in equations 3 and 4. The source follower gain is mainly degraded by the body effect because the source-body trans-conductance term ($g_{mb}$) dominates over the smaller source-drain conductance ($g_{ds}$) of *M1* and *M2*. The simulated value of the source follower gain is $A_{vSF} = 0,815$. $g_{m3}$ depends on the size of M3 and its biasing current and is equal to 7.3 *mS*. Finally, the current mirror gain is degraded due to the CLM effect and is equal to 3,66, in comparison with the theoretical value of approximately 50/12=4,16. The sensor gain therefore is equal to

$$\qquad (8)$$

$$G = 0.815V \cdot 0.0073\frac{A}{V} \cdot 3.66 \cdot 50\Omega = 1.1 \cong 1.1dB$$
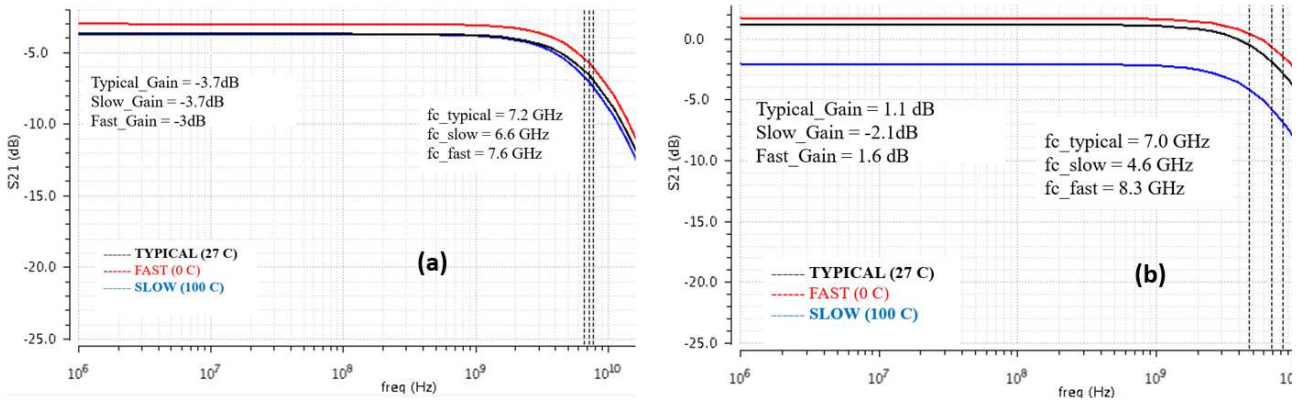


Fig. 5    S21 parameter for PT variations of the (a) Bulk driven MOSFET sensors and the (b) Source Follower – Trans-conductor (SF+Gm)
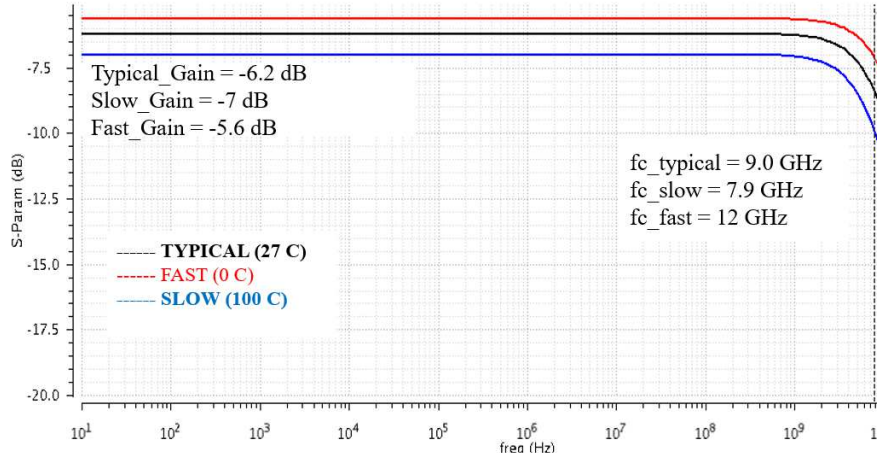
Fig. 6    S21 parameter for PT variations of the DC Coupled supply monitoring sensor

The sensor frequency response is depicted in Fig. 5(b). It has a low but adequate gain and relatively high *BW*. However, its performance cannot be significantly improved without impractical power consumption. Similarly to the bulk-driven sensor, it suffers from signal contamination, due to its single-ended output. It is compact and can be used on complex chips because the output current can be easily multiplexed using pass transistors.

The *DC* coupled sensor gain-*BW* performance is provided in Fig.6. The gain of this sensor is below unity because it is actually composed of two source followers on each signal: one source follower that senses the differential signal and a second one that acts as buffer to match the 50Ω impedance of the transmission line. Therefore, no stage with gain>1 is used. This is the most significant disadvantage of this monitoring method. The *BW* is high partially due to the low gain. Because it is a symmetrical design, statistical mismatch variations are subtle. Without the buffers it consumes low area. The buffers need to be wide to achieve an output resistance of 50 Ω and therefore consume more area.

The overall sensors performance versus gain-bandwidth, including process and temperature variations, is given in table II. The respective linearity performance in terms of the 1dB compression point is depicted together with the power consumption and the overall occupied active area. The bulk driven sensor is the most efficient in terms of active area, consuming only 180 $\mu$m². The bandwidth is not the best, but competitive to the rest and its linearity is the highest reaching 980 mV. The respective gain is quite low in the range of -3.7 dB. The *SF-g$_m$* sensor has a comparable *BW* of 7 GHz, but its gain is higher reaching 1.1 dB. The 1dB compression point is the worst among the simulated sensors, equal to 130 mV. In relation to the area, this sensor has a medium figure of 570 $\mu$m². Finally, the DC coupled sensor has a low gain of -6.2 dB, but the highest *BW* equal to 9 GHz, appearing as the most advantageous for high frequency monitoring. On the other hand, it occupies the largest area and its linearity is moderate compared to the Bulk driven topology.

TABLE II.    SENSORS PERFORMANCE

| Ground Bounce Sensors | | | |
|---|---|---|---|
| Performance | Bulk Driven MOSFET | SF-gm Follower | DC Coupled PMOS Sensor |
| Gain | -3.7 dB | 1.1 dB | -6.2 dB |
| Gain PT variation | -3 to -3.7 dB | -2.1 to 1.6 dB | -7 to -5. 6dB |
| Bandwidth | 7.2 GHz | 7 GHz | 9 GHz |
| Power Consumption | 8.3 mW | 11 mW | 6.8 mW |
| 1dB Comp. Point | 980 mV | 130 mV | 280 mV |
| Active Area | 180 $\mu$m² | 570 $\mu$m² | 930 $\mu$m² |

## IV. SUMMARY

Three compact, ground bounce sensors were presented. They are analyzed topology wise, designed in a 65 *n*m *RFCMOS* process, and extensively simulated. Specific criteria were extracted in relation to the suitability of each sensor versus the SoC application. The bulk driven MOSFET sensor is the most compact and linear one but with no option for output multiplexing and medium *BW*. The SF-gm sensor has the highest gain but with limited linearity and *BW*. Finally the *DC* coupled sensor has the highest *BW*, but its gain is low and requires the largest area.

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