An LVPECL-based Phase-Frequency Detector with 15 ps Dead Zone in 130 nm SiGe BiCMOS

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***Abstract*—A high-speed phase-frequency detector (PFD) based on low-voltage positive emitter-coupled logic realized in a 130 nm SiGe BiCMOS technology is investigated in this research work. It is intended for providing accurate and fast phase tracking to synchronize a network of decentralized clocks. With a dead zone of around 15 ps, which equals a precision of 5° at 1 GHz for symmetrical square wave signals, and no blind zone the PFD is among the fastest reported, while also operating very robustly.**

***Index Terms*—phase-frequency detector, low-voltage positive emitter-coupled logic, dead zone, BiCMOS integrated circuits**

I. Introduction

Clock synchronization is a recurring challenge in modern electronics. In this context, phase-locked loops (PLLs) are mainly used to enable accurate synchronization of high-frequency oscillators based on precise reference clocks [1]. One of the main components in such negative feedback control loops is the phase detector (PD) or phase-frequency detector (PFD). While PDs can only detect differences in phase, PFDs offer the ability to detect phase as well as frequency differences simultaneously and thus reduce the PLL's locking time.

The synchronization of spatially distributed clocks is a problem in many applications. For example, most communication protocols implement regular pilot sequences to synchronize the time base of every client. A completely new approach can be found in the current research context of synchronization of spatially separated mutually delay coupled PLL systems [2]–[4]. For such approaches, accurate synchronization requires a very precise detection of phase differences between two input signals. High coupling frequencies between the nodes and fast response times of the phase detection circuitries have been shown to be beneficial for accurate synchronization in the presence of pertubations.

The PLL system used for mutually coupled oscillator nodes is shown in Fig. 1. A charge pump (CP) subsequent to the PFD transforms the two digital PFD output signals into an analog output current i_c, which is in turn converted to a suitable voltage-controlled oscillator (VCO) control voltage u_c by a loop filter (LF) to make the VCO adjust its instantaneous output frequency. The VCO output is divided by an integer factor N using a frequency divider (FD) and fed back to the second input of the PFD, denoted by index 2 in Fig. 1, as well as to other coupled PLL nodes [4]. The first input signal of the PFD is in turn equal to the output of another node's divided

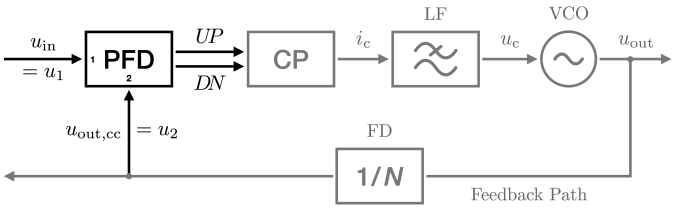


Fig. 1. Block diagram of a PLL system with phase-frequency detector (PFD) as well as charge pump (CP), loop filter (LF), voltage-controlled oscillator (VCO) and frequency divider (FD). This architecture is used in the context of synchronization of mutually coupled PLLs. Hence, a capability of cross coupling of the feeback signal $u_\mathrm{out,cc}$ to another node is implemented.

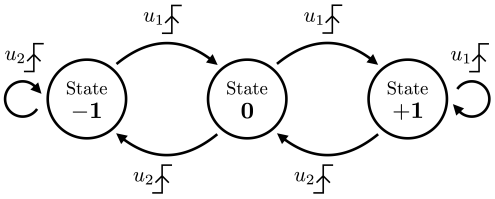
VCO frequency delayed by the transmission delay between the two nodes.

In order to ensure a seamless transition with existing hardware for mutually coupled nodes [5], the PFD must be capable of interfacing with low-voltage positive emitter-coupled logic (LVPECL). This signal standard is based on differential pulses and provides optimized interfacing between components at high clock rates up to single-digit GHz frequencies. Hence, the PFD's input signals are expressed using symmetrical square wave signals $u_1(t) = \hat{U}_1 \operatorname{rect}(\omega_1 t + \varphi_1)$ and $u_2(t) = \hat{U}_2 \operatorname{rect}(\omega_2 t + \varphi_2)$. They are compared in terms of phase Eq. (1) and frequency Eq. (2), where $\omega = 2\pi f$:

$$\Delta\varphi(t) = \varphi_2(t) - \varphi_1(t), \tag{1}$$

$$\Delta\omega(t) = \omega_2(t) - \omega_1(t). \tag{2}$$

Taking advantage of the fundamental relationship of frequency error resulting in an accumulation of phase error over time, the PFD is able to react to both quantities by acting on the number and timing of encountered positive (or negative) signal edges of the input signals. Two differential output signals called *UP* and *DN*, the naming of which already suggests their effect on shifting VCO frequency, assume states according to Fig. 2. Compared to conventional XOR type phase detectors without means of frequency detection and with a phase tracking capability of only $|\Delta\varphi| = \pi\,/\,2$, the PFD's $|\Delta\varphi| = 2\pi$ periodical behavior according to its underlying state machine of Fig. 2 promises even faster acquisition of an unambiguous, stable locking state for coupled oscillators across an almost unlimited tracking range. Only for very closely aligned signal edges on the two inputs, a PFD might



State	*UP*	*DN*
-1	0	1
0	0	0
$+1$	1	0

Fig. 2. PFD state machine, based on [1]. States result from a ternary output signal constellation of *UP* and *DN*. The fourth conceivable state of both *UP* and *DN* being active at the same time is prohibited by an internal reset signal.

not be able to detect the according phase offset anymore. This is because for a PFD to exhibit the desired behavior of Fig. 2, reset signals are necessary to clear the memory elements within the PFD architecture, which due to internal delays will mask *UP* and *DN* at some point. This effect, which determines PFD operating precision and thus also speed (implying suitability for high frequency input signals), is described by a so-called dead zone and determines PLL phase noise (or jitter in time domain). Compensation can be done by adding a delay element to the reset path resulting in both *UP* and *DN* being regularly active at the same time for an exactly known duration, also periodically in locked condition [6]. However, this will introduce so-called reference spurs to the PLL output spectrum and give rise to the problem of blind zone, where during the deliberately extended reset periods an occurrence of a signal edge might be missed resulting in opposite-to-intended PFD output behavior (e.g. *UP* signals instead of *DN* signals) [7]. Apart from these challenges, recent PFD research mainly evolved around optimizing CMOS designs for minimum transistor count, layout area and power consumption, e.g. [8].

The aim of this work is to investigate and individually characterize a high-speed PFD realized without dead zone compensation, thus avoiding blind zones, by building upon a very fast bipolar logic instead of intentional delays.

II. Circuit Design

In order to realize the state machine shown in Fig. 2, the architecture shown in Fig. 3 based on two D-flipflops and an AND gate is used [1], [9], [10].

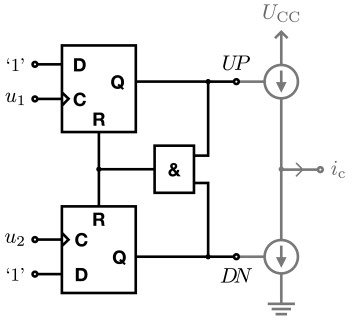


Fig. 3. PFD logic block architecture. (The subsequent charge pump doesn't fall within the scope of this work and is therefore marked in gray.)

To provide the required rising edge triggered D-flipflop, two of the D-latches shown in Fig. 4 are put in series to act as a master-slave arrangement with complementary clock inputs restricting the signal passing to rising signal edges only with signal holding inbetween. An asynchronous reset functionality is added to the two D-flipflops so, in accordance with Fig. 2, a prohibited state of both *UP* and *DN* being high at the same time can be prevented by AND-combining them, instantaneously resetting both flipflops.

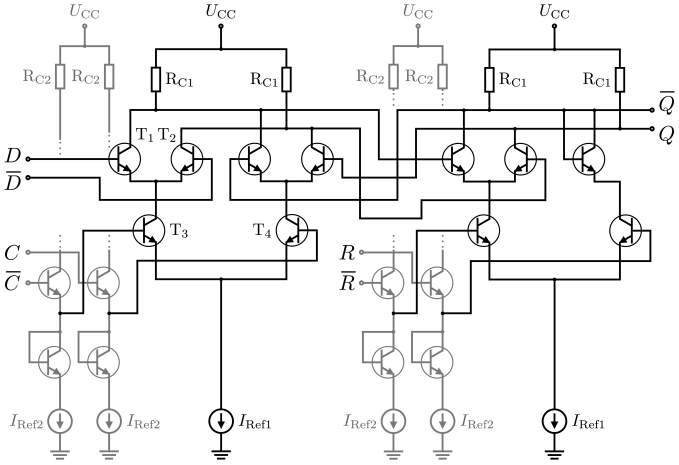


Fig. 4. Simplified schematic of the implemented master D-latch of a master-slave D-flipflop consisting of interleaved differential pair arrangements and level shifters (marked in gray). An input signal D is passed along to the output Q when the clock C is active low. The PFD topology also requires an asynchronous reset capability R.

In accordance with a robust fully differential nature of the design, switching elements are realized as differential pairs based on two bipolar junction transistors (e.g. T_1 and T_2 in Fig. 4) to steer a current predefined by a current source at the common emitter through one of the two collector resistors (denoted R_{C1} in Fig. 4) to obtain a voltage drop of $800\,\mathrm{mV}$ at the respective output node, with the other collector output node of the pair providing the inverted signal. With a supply voltage of $U_{CC} = 3.3\,\mathrm{V}$, the desired logic levels are $U_{high} = 3.3\,\mathrm{V}$ and $U_{low} = 2.5\,\mathrm{V}$ with a common-mode voltage of $U_{CM} = 2.9\,\mathrm{V}$ inbetween, which can be used for single-ended termination of differential pairs or logic blocks. Approximately $U_{diff} = 200\,\mathrm{mV}$ of signal amplitude are required to completely switch a stage. LVPECL differential pairs are interleaved for more complex logic blocks, with input level shifting required for the outer pairs (e.g. T_3 and T_4 in Fig. 4) to ensure favorable high-speed operating points for all transistors while under all conditions obeying restrictions in terms of e.g. maximum allowed collector-emitter voltages.

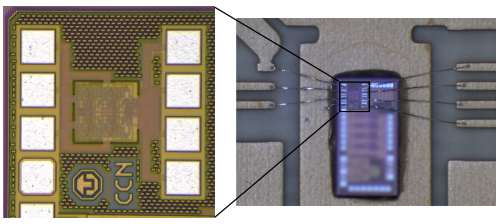


Fig. 5. Photo of the fabricated PFD with pads for bonding to a printed circuit board for individual characterization.

To prove the feasibility of the concept, the circuit was implemented in a 130 nm SiGe BiCMOS technology providing a transit frequency f_t of 300 GHz. A compact integrated circuit layout with a total of 118 NPN transistors was realized on an active area of 150.5 µm × 143 µm, Fig. 5. *UP* and *DN* signal paths were routed in a strictly symmetrical manner to avoid internal delay asymmetries. To save the space which would be required for two additional pads, the differential inputs were terminated on-chip for single-ended operation. For measurement purposes, the PFD was bonded to a printed circuit board (PCB) using a high-frequency substrate, shown in Fig. 5.

III. Simulation and Measurement

To prove the concept, the integrated circuit was experimentally measured in the laboratory. For functional time-domain characterization of the PFD, a measurement setup of two synchronized *Keysight 33600A Series* waveform generators (WG) and a *Rohde & Schwarz RTO2044* oscilloscope was implemented, Fig. 6. After performing a zero-phase calibration routine (also compensating for cable lengths) and taking advantage of the waveform generators' mutual frequency synchronization capability, the output signal of the first WG is held fixed while the phase offset of the second WG's output signal is swept. This is done automatically by a measurement script at fequencies of up to 1 MHz. This frequency was intentionally chosen, because input square wave signals of a sufficiently steep edge are still available. In accordance with the LVPECL standard, the IC is supplied with a supply voltage of 3.3 V. It consumes a total current of 21.6 mA, independent of its state of operation. The total DC power consumption is 71.3 mW including all reference currents.

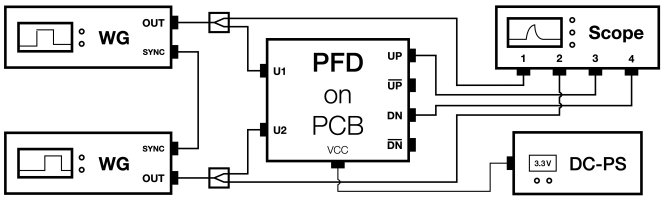


Fig. 6. Measurement setup used to characterize the PFD, including waveform generators (WG), oscillosope (Scope) and DC power supply (DC-PS).

The upper plot in Fig. 7 shows the measured behavior of the PFD for two square wave input signals at frequencies of 1 MHz. Both signals U_1 and U_2 are phase-locked with a constant offset $\Delta\varphi$ of 90°, which implies that U_1 leads U_2. The corresponding signal of the PFD at the *UP* output is shown in the middle diagram, while the *DN* output is given in the bottom diagram. A correct behavior of the *UP* and *DN* outputs of the PFD can be observed at this given phase difference $\Delta\varphi$: The logic level of signal *DN* remains low while the *UP* signal simultaneously delivers a high pulse of a width exactly corresponding to the input phase difference. In the case that the rising edge of signal U_1 is lagging U_2 by 90° at the same frequency of 1 MHz, the PFD output *UP* remains low, while

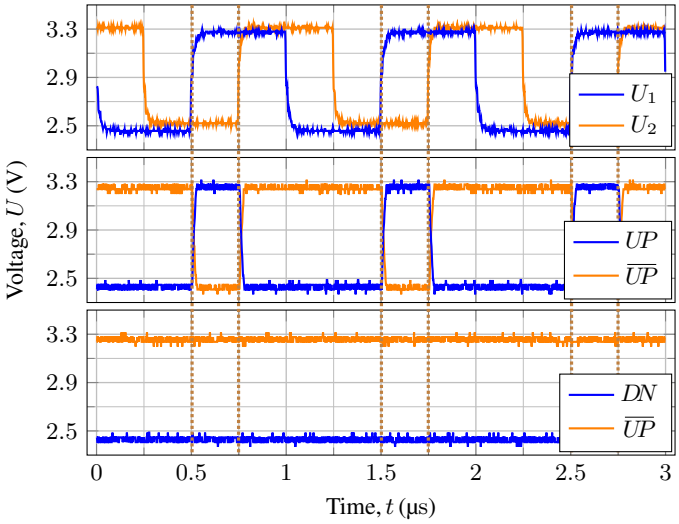


Fig. 7. Measured PFD signals for an exemplary input phase offset of $\Delta\varphi = 90°$ at identical frequencies of $f_1 = f_2 = 1$ MHz. A positive signal flank was encountered on U_1 first. So *UP* pulses are proportional to the phase difference between the input signals. In this figure, dotted lines are drawn where the input signals cross U_{CM} to show the propagation delay of the output signals.

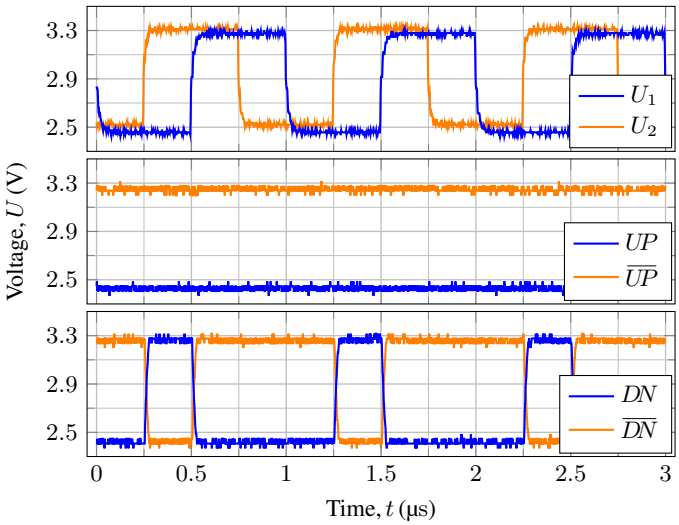


Fig. 8. Measured PFD signals for an exemplary input phase offset of $\Delta\varphi = -90°$ at identical frequencies of $f_1 = f_2 = 1$ MHz. A positive signal flank was encountered on U_2 first. So *DN* pulses are proportional to the phase difference between the input signals.

the pulses at the *DN* output correspond to the phase difference of the input signals, as shown in Fig. 8.

Shifting phase offsets from -720° to 720°, the output waveforms *UP* and *DN* can be combined by integration over a signal period and subtraction according to Eq. 3 to anticipate the behavior of the charge pump providing a control current i_c:

$$i_c(t) \propto \int_{t=0}^{t=T} UP(t)\,\mathrm{d}t - \int_{t=0}^{t=T} DN(t)\,\mathrm{d}t. \qquad (3)$$

This yields the PFD's transfer curve in Fig. 9. The tracking characteristic is linear as intended with some minor dead zone related flattenig apparent around $\Delta\varphi = 0$.

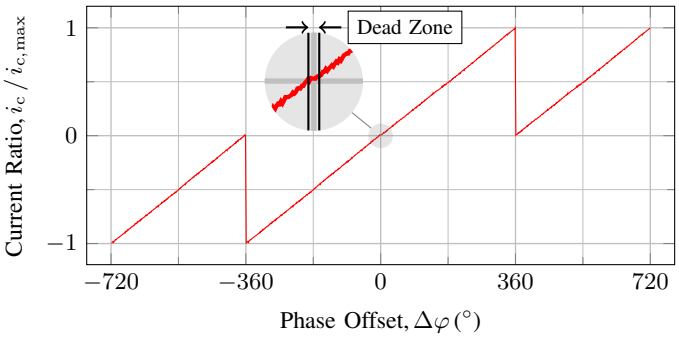


Fig. 9. Measured PFD transfer curve for symmetrical square wave signals at 1 MHz, expressed as a charge pump current ratio $i_c / i_{c,max}$ according to Eq. 3. A minor dead zone is visible in the form of flattening around $\Delta\varphi = 0$.

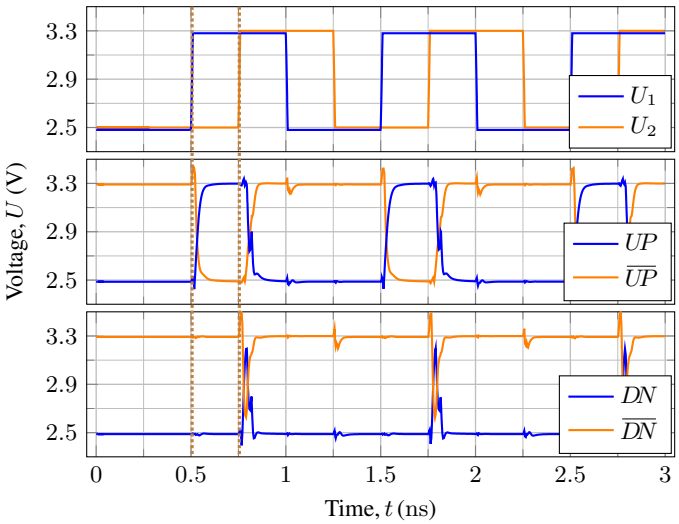


Fig. 10. Simulated PFD signals for an input phase offset of $\Delta\varphi = 90°$ at identical frequencies of $f_1 = f_2 = 1\,\text{GHz}$. A positive signal flank was encountered on U_1 first. So *UP* pulses are proportional to the phase difference between the input signals. Reset pulses are apparent on the inactive output *DN*.

For comparison, the simulated PFD performance was also investigated using finite element time-domain simulation including all parasitics of the layout. The result, shown in Fig. 10, reveals that the limiting factor in terms of precision is the reset pulse, which at a certain minimum detectable phase offset will mask *UP* and *DN*. At it's base, it is 57 ps wide. However, output pulses are still distinctively larger in terms of area under the curve while still reaching full logic levels to turn on the charge pump with according integration consistently yielding clear results for *UP* and *DN* pulsed behavior down to 10 -15 ps. This dead zone equals a PFD phase resolution of e.g. 0.005° at 1 MHz or 5° at 1 GHz or 90° at 18 GHz. In the latter regard, it is e.g. 7.2-times faster than the speed-oriented ("no dead zone") CMOS design of [8], which however uses less transistors and only consumes a power of 6.6 µW at 1.8 V. A benefit of not compensating for the PFD's small dead zone is that there is no blind zone. The propagation delay is also low with the PFD exhibiting an output reaction after 19 ps and reaching the U_{CM} level after 35 ps. The 10-90% rise / fall time is at approximately 39 ps, 5.6-times faster than the fastest emitter-coupled logic PFD found [11].

The PFD proved in simulation and measurement to work nominal with distorted, noisy or asymmetrical differential input signals as long as the desired logic state at an input is reliably conveyed as a voltage difference of at least $U_{diff} = 200\,\text{mV}$. Additionally, the PFD proved to work reliably at supply voltages down to $U_{CC} = 2.5\,\text{V}$.

Conclusion

The phase-frequency detector (PFD) circuit investigated in this feasibility study is designed to work as part of a phase-locked loop (PLL) within a network of mutually delay-coupled spatially distributed non-hierarchical oscillators. It allows a seamless integration with existing hardware due to its compatibility with low-voltage positive emitter-coupled logic interfaces. Compared to other research works, it has a dead zone of only 15 ps, which equals a phase tracking precision of 5° at 1 GHz for square wave signals. The PFD design provides a very fast and robust tracking operation.

Acknowledgment

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