A novel current sensing technique for photovoltaic MPPT applications

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***Abstract*— In this paper an improved current sensing technique suitable for DC-DC Boost converter is proposed. Its principle of operation is based on exploiting the DC resistance (R_{DCR}) of the input inductor L to detect the input current by sensing the voltage drop across it. A highly linear differential G_m-transconductor and a V-I converter along with a current integrator are utilized to further process this voltage drop and produce a square-wave pulse signal with its frequency proportional to the input current. The current sensor circuit has been designed and fabricated in 180nm XFAB technology and simulation results over PVT corners exhibits a frequency operation range 3kHz-90kHz and worst-case frequency linearity error of 6.4%.**

Keywords—photovoltaic MPPT applications, lossless current sensing, integrated circuit, current-to-frequency converter

I. INTRODUCTION

The utilization of renewable energy sources is rapidly evolving which is reflected in both research and the electronics industry. Solar energy is considered an alternative source of electricity that is very promising due to its various positive features; it is highly available, pollution-free and its maintenance is arguably cost-effective.

Nevertheless, several factors should be taken into consideration and addressed to regard solar energy as an efficient alternative renewable energy source. Photovoltaic cells are characterized by a low conversion efficiency, which significantly diminishes the overall system efficiency. Furthermore, the combination of the nonlinear physical characteristic of the solar cell and the dependence of the maximum power provided by the cell from rather unpredictable irradiation level as well as the ambient temperature [1], rises the need for techniques that harvest the maximum available energy from photovoltaic panels under all conditions (Maximum Power Point Tracking, MPPT).

A common MPPT practice is the utilization of a DC-DC converter between the PV panel and the load or a battery, where the former is controlled by the MPPT unit to achieve the maximum available power from the PV cell and deliver it to the latter.

II. MPPT METHODS IN PHOTOVOLTAIC ENERGY HARVESTING APPLICATIONS

A. MPPT Algorithms

Maximum Power Point Tracking (MPPT) is an algorithm that ensures that the PV system operates utilizing most of the available power, regardless of the operating and the ever-changing environmental conditions (partial shading, solar irradiation level, temperature, and load).

The two predominant MPPT algorithms are the Perturb and Observe (P&O) method and the Incremental Conductance (IncCond) method. Their main operation is to sample the operating points and adjust the impedance seen by the solar cell or array, by regulating the duty cycle of the DC-DC converter [2].

The P&O method senses the output current and voltage of the PV panel to calculate its output power and compares the present and past value of this power to adjust the duty-cycle accordingly. The IncCond method is based on the principle that the slope of the PV array curve is zero at the Maximum Power Point, so that $\Delta P/\Delta V = 0$, with $P = VI$. The MPP can be tracked by comparing the instantaneous conductance I/V with the incremental conductance $\Delta I/\Delta V$ [3].

Both methods require the acquisition of the PV panel's output voltage and current values to determine the Maximum Power Point. Therefore, the need for voltage and current sensing methods that efficiently and accurately extract information on these values lead to the development of techniques, some of which are described in the next subsection.

B. Current sensing techniques

While voltage sensing is generally a non-complex process, current sensing poses several challenges, due to its invasive nature that often requires a resistive element added in series to the input inductor of the DC-DC boost converter. The voltage drop on this resistor is proportional to the input current and can be sensed by an amplifier. The main drawback of this method is the power dissipation caused by the series resistance, which is proportional to its value times the square of the input current and reduces the overall power efficiency.

Another method exploits the on-resistance of the DC-DC converter's power MOSFET, by sensing the drain-source voltage, V_{DS}. While this technique is lossless, since no additional resistance is needed, it has the disadvantage of providing current information only for the duration that the MOSFET is on [4].

Another technique that involves the power MOSFET is the use of a SenseFET, which is a MOSFET that forms a current mirror with the original power MOSFET and provides a scaled version of the desired current.

Various methods utilize the inductor of the DC-DC converter and specifically its DC resistance. Filtering the

voltage using an RC filter and then measuring the voltage drop on the inductor, provides a voltage value proportional to the input current [5]. This technique is lossless since it exploits the existing dc resistance of the inductor without adding extra passive element and thus there is no impact on the power efficiency performance. In addition, most of the aforementioned voltage and current sensing methods involve Analog-to-Digital Converters (ADCs) to convert the signal from the analog to the digital domain. This significantly impacts the system complexity and results in increased power consumption [6][7].

C. *Brief description of the proposed circuit*

The topology of the proposed current sensor is presented in Fig. *1*.

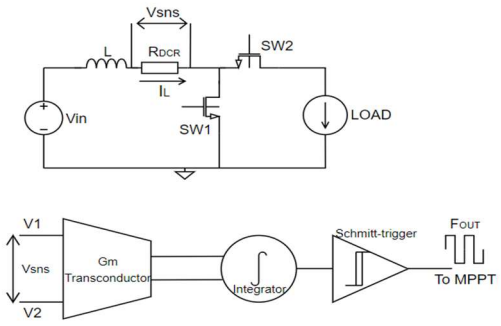

Fig. 1. (a) Boost Converter architecture (b) Block diagram of the proposed current sensor.

The key idea behind the proposed circuit, which is based on [8], is that it offers the detection of the input current I_L on the DCR inductor resistance and its conversion to a voltage difference. This voltage drop, $V_{sns}=I_L \cdot R_{DCR}$, is converted through the subsequent stages of the current sensor, into a sequence of square pulses with their frequency proportional to the magnitude of the input current. This approach has two main advantages: it does not make use of an additional resistor connected in series with the inductor, which would lead to extra power losses. On the other hand, there is no need of an Analog-to-Digital converter to translate the analog current information and proceed it to the digital part of the whole system, because the output square pulses have already carried this information.

Its operation principle is described in the following: the input current I_L of the boost converter (Fig.1a), which flows through the inductor resistor R_{DCR}, creates a voltage drop V_{sns} across it. This voltage difference is sensed and applied at the input of the linear G_m transconductor. The transconductor differential output current is amplified by the V-I converter and is fed into a bidirectional integrator which is driven by a Schmitt trigger comparator. The frequency of the output signal is proportional to the input sense voltage and is given by the following equation:

$$F_{OUT} \sim \frac{V_{sns}}{C(V_{ch}+V_{dis})} \qquad (1)$$

where F_{out} denotes the output frequency, V_{sns} the sense voltage across the DCR inductor resistance, and C, V_{ch}, V_{dis} are referred to the capacitor value, charge, and discharge voltage levels inside the integrator, respectively. In the next section a detailed description of the individual circuit blocks of the proposed current sensor will be given.

III. Proposed Current Sensing Circuit

A. *Circuit description – I/F*

In Fig. 2 is depicted the first block of the chain which is a CMOS differential transconductor with resistive degeneration. Due to its good linearity performance and differential configuration, it becomes successfully appropriate for our implementation. The two inputs of the opamps, V_1 and V_2, are connected between the terminal nodes of the R_{DCR} to sense V_{sns} voltage. Due to the negative feedback, the current, that flows through the resistor R, is related to the two input voltages by (2):

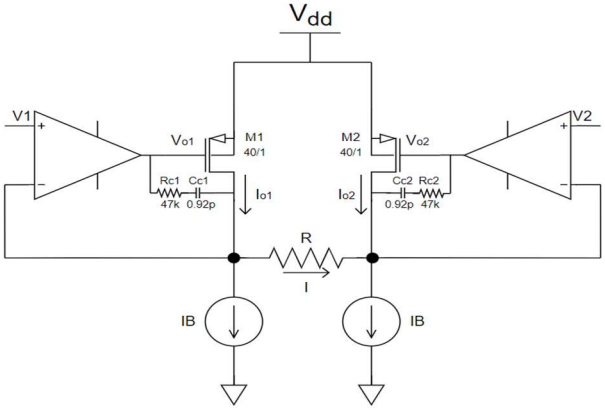

Fig. 2. G_m-Linear differential transconductor

$$I = \frac{V_1 - V_2}{R} \qquad (2)$$

Assuming that transistors *M1* and *M2* have the same transconductance $g_{m1}=g_{m2}=g_m$, and also taking into account that $I_{o1}=g_{m1}V_{o1}$ $I_{o2}=g_{m2}V_{o2}$, the difference V_{o1}-V_{o2} of the two output voltages of the opamps is given by:

$$V_{o1} - V_{o2} = \frac{2}{g_m R}(V_1 - V_2) \qquad (3)$$

This voltage difference is applied to the next stage of the current sensor, which is the differential *V-I* converter. The two opamps are designed for low current consumption and the passive elements R_{ci},C_{ci} (i=1,2) ensures sufficient phase margin for stability purposes. The resistor *R* value has been chosen to be around 600kΩ, compromising linearity and occupied layout chip area. The *IB* constant bias current is 500nA.

The differential *V-I* converter in combination with the bidirectional integrator is presented in Fig. *3*. As it can be seen, the circuit is fully symmetrical having as input the V_{o1} voltage at the left side and the V_{o2} voltage at the right side.

Transistors *MP1* and *MP3* should have equal aspect ratio with *M1* and *M2* of the G_m-transconductor to generate the same output currents I_{o1} and I_{o2} respectively. The functional operation of this circuit is analyzed in the following:

During the charge phase of the capacitor *C*, PMOS switch transistor *MPS1* is on, while NMOS switch *MNS1* is off.

The I_{chp} current is equal to:

$$I_{chp}=I_{MP2}+I_{MPb3} \qquad (4)$$

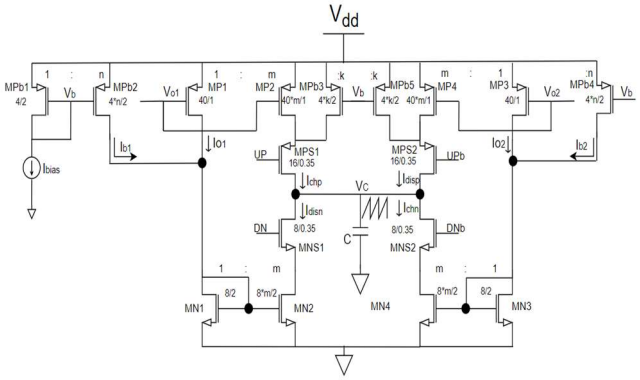

Fig. 3. V-I Converter and bidirectional integrator

where I_{MP2} is m times higher than I_{o1} and I_{MPb3} is a replica of I_{bias} with a scaling factor of k. So, (4) can be rewritten as:

$$I_{chp}=mI_{o1}+ kI_{bias} \qquad (5)$$

On the right side of the circuit, PMOS switch transistor *MPS2* is off and NMOS switch *MNS2* is on and the current I_{chn} is given by (6):

$$I_{chn}=I_{MN4} =m(I_{o2}+nI_{bias}) =mI_{o2}+m\cdot nI_{bias} \quad (6)$$

The net charging current to the capacitor is simply the difference between I_{chp} and I_{chn}:

$$I_{ch}=I_{chp}-I_{chn}=m(I_{o1}-I_{o2}) \qquad (7)$$

which implies that the scaling factor *k* should be equal to the product of the two other current mirror scaling factors *m* and *n*. When the capacitor voltage V_C reaches the high threshold voltage level V_H of the Schmitt trigger comparator (Fig. *4*), its output *OUT* toggles from high to low and initiates the discharging phase. *UPb* and *DN* signals change polarity and activate the PMOS and NMOS switches, *MPS2* and *MNS1,* respectively. Applying a corresponding calculating approach for the discharging phase of the capacitor, the I_{dis} current is given by:

$$I_{dis}=I_{disp}-I_{disn}= m(I_{o2}-I_{o1}) \quad (8)$$

which is like (7), but with opposite polarity of the current difference. Once the capacitor voltage V_C reaches the low threshold voltage level V_L, comparator's output toggles from low to high and the procedure starts again. In this way, a repeated charge and discharge loop is built up with a frequency of oscillation given by:

$$F_{OUT} = \frac{\Delta I_o}{C(V_H+V_L)} \qquad (9)$$

Since ΔI_o is proportional to the voltage difference V_{sns} across the inductor R_{DCR} resistance, it is emerging from (9) the linear relationship between F_{out} and V_{sns}.

The corresponding scaling current ratio values *k, m* and *n* are 20, 4 and 5 respectively and the I_{bias}=50nA. All the transistors used in the current mirrors have channel length 2um to reduce second order effects such as channel length modulation. Switches *MPS1-MPS2-MNS1-MNS2* have minimum channel length (350nm) to minimize the R_{on} resistance and the V_{ds} voltage across them. The integrating capacitor *C* has been implemented by a MIM capacitor and its value is ~13pF.

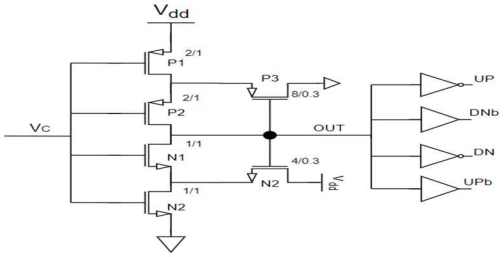

Fig. 4. Schmitt-trigger comparator

IV. TESTBENCH

The testbench that was used to test the functionality of the circuit is illustrated in Fig. *5*. It includes a DC-DC boost converter and a low-pass filter (LPF), which is connected at the right node V_2 of the input inductor. Since at this node the signal is a square-like waveform created from the alternate switching of the power MOSFETs, the low-pass filter is implemented to filter out the switching frequency of the DC-DC converter from the signal.

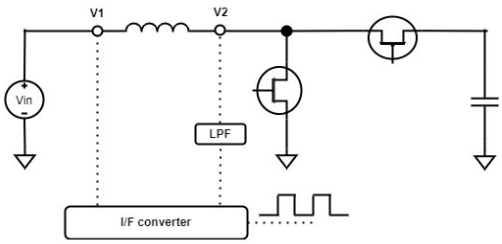

Fig. 5. Simulation testbench for the I-F converter

The voltage V_2, after the filtering process, has a value equal to the input voltage of the DC-DC converter, V_1, minus the voltage drop V_{sns} across the inductor's DC resistance R_{DCR}. This voltage drop is proportional to the input current.

$$V_2 = V_1 - V_{sns} = V_1 - I_{in}R_{DCR}$$
$$\rightarrow \Delta V = V_1 - V_2 = I_{in}R_{DCR}$$

Therefore, measuring the voltage difference ΔV provides a value that is proportional to the input current. The specifications of the system that have been used in the testbench are listed in Table 1.

Table 1. System specifications

Testbench specifications		
Parameter	***Value***	***Unit***
Input inductor, L_{in}	100	μH
Inductor DC resistance, R_{DCR}	50	mΩ
Output capacitor, C_{out}	66	μF
Switching frequency, f_{sw}	50	kHz
Low-pass filter resistor, R_{LPF}	100	MΩ
Low-pass filter capacitor, C_{LPF}	50	pF
Input current range, I_{in}	0-2	A
Input voltage range, V_{in}	0-1.4	V

V. SIMULATIONS

The proposed current-to-frequency converter has been designed in a 0.18 μm XFAB CMOS technology with a nominal supply voltage 2.3V. All circuits have been implemented by using 3.6V devices and the temperature ranges from 0 to 80ºC. The occupied layout area on the silicon is 270umx300um.

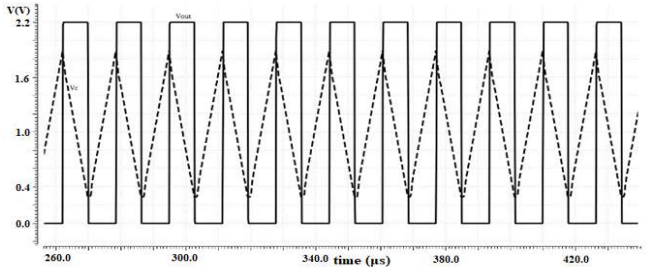

Fig. 6. Output Vout (square) and voltage (triangular) capacitor *Vc* for V_1=0.8V

Fig. 6 shows the waveform of the I-F converter output V_{out} and V_c in the time domain for V_1=0.8V. The transient parametric simulation results of the F_{out} versus V_2 voltage for V_1=0.3V, 0.5V, 0.8V, 1.1V and 1.4V indicative voltages are presented in Fig.7. The slope $\Delta F/\Delta V_2$ for each V_1 voltage is constant and the minimum and maximum frequencies are 4.3kHz and 68.7kHz, respectively. The power consumption amounts to 150μW.

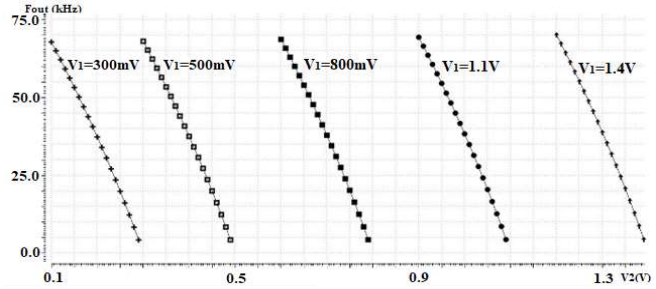

Fig. 7. F_{out} vs V_2 for various V_1 voltages

In Fig. 8 the simulation results over PVT corners of the output frequency F_{out} versus the input voltage difference V_1-V_2 are illustrated. The temperature and the supply voltage variations are 0-80ºC and 2.2V-2.4V, respectively. As it can be observed, the output frequency range spans from 3kHz-90kHz for an input voltage range of roughly 150mV. The duty cycle of the output signal ranges from 37% up to 52% with a nominal value of 48.7%.

The plotted trace with circle symbols corresponds to the nominal case and the one with the box symbols to the worst-case corner from a linearity perspective. The circuit exhibits a linearity error (1-sigma deviation) of 0.8% for the nominal and 6.4% for the worst case.

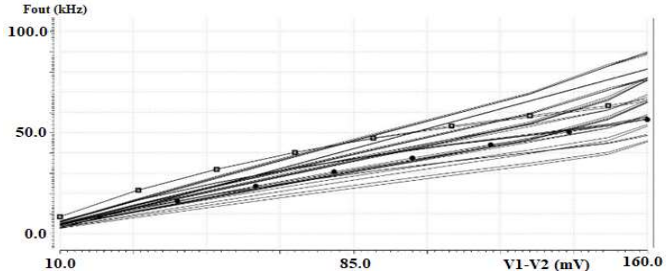

Fig. 8. F_{out} (kHz) vs $\Delta V=V_1-V_2$ (mV) over PVT corners

VI. CONCLUSIONS

The current sensing technique employing a novel current-to-frequency converter that is presented in this paper achieves an adequate F_{out}-I_{in} linearity and therefore it can efficiently extract information on the input current of a DC-DC converter. Along with a voltage-to-frequency converter like the one presented in [8], both current and voltage information can be extracted and transformed into digital signals, providing the necessary data to an MPPT algorithm to be used in photovoltaic applications.

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REFERENCES

[1] Yang, Chih-Yu et al. "Highly efficient analog Maximum Power Point Tracking (AMPPT) in a photovoltaic system," IEEE Transactions on Circuits and Systems I: Regular Papers 59 pp. 1546-1556, 2012.

[2] M. Hlaili, M. Hfaiedh, "Comparison of different MPPT algorithms with a proposed one using a power estimator for grid connected PV systems," International Journal of Photoenergy, pp. 1-10, 2016.

[3] M. W. Rahman, C. Bathina, V. Karthikeyan and R. Prasanth, "Comparative analysis of developed incremental conductance (IC) and perturb & observe (P&O) MPPT algorithm for photovoltaic applications," 10th International Conference on Intelligent Systems and Control (ISCO), pp. 1-6, 2016.

[4] C. -W. Hsu, K. -P. Chiu and J. -F. Chen, "The Vds signal of power switch for boost PFC current detection," IEEE 4th International Future Energy Electronics Conference (IFEEC), pp. 1-6, 2019.

[5] B. X. Li, K. S. Low and B. Y. Kang, "An accurate lossless current sensing approach for a DC-DC converter with online calibration," 2014 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC), pp. 1-5, 2014.

[6] E. Koutroulis and F. Blaabjerg, "A new technique for tracking the Global Maximum Power Point of PV arrays operating under partial-shading conditions," IEEE Journal of Photovoltaics, vol. 2, no. 2, pp. 184-190, April 2012.

[7] K. S. Tey and S. Mekhilef, "Modified Incremental Conductance algorithm for photovoltaic system under partial shading conditions and load variation," IEEE Transactions on Industrial Electronics, vol. 61, no. 10, pp. 5384-5392, Oct. 2014.

[8] C. Azcona, B. Calvo, N. Medrano, S. Celma and M. R. Valero, "A CMOS micropower voltage-to-frequency converter for portable applications," 7th Conference on Ph.D. Research in Microelectronics and Electronics, pp. 141-144, 2011