A low power low noise 65nm charge pump using mismatch compensation and smoothing capacitor

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***Abstract*—This work presents a Charge Pump circuit using active current mismatch compensation, which exhibits low power, low noise and good linearity for integer or fractional -N PLL. The proposed charge pump has a V_{ctrl} range of 0.3V to 0.75V, $1.135\ x\ 10^{-24} A^2/Hz$ output current noise and current mismatch below 0.01%. Additionally, it includes a smoothing capacitor to reduce the transient phenomena which generate non-linearity. The layout dimensions of the proposed charge pump is 88um x 80um. Finally, the charge pump is designed using 65nm TSMC process with a supply voltage of 1V and power consumption of 309uW at 150uA current output.**

Keywords— PLL, Charge Pump, Current Mismatch, Linearity, Low Noise, Low Power

I. Introduction

Phase locked loops play a significant role to modern chip industry and more specifically, high frequency PLLs with low jitter, low power consumption and small die area. Frequency synthesizers are used in many applications like WiFi, Bluetooth, RF transmitters and receivers and CDRs. Charge pump's performance is crucial to the overall behavior of a PLL and its critical aspects are V_{ctrl} range, current mismatch, linearity, low phase noise and current variation over process and temperature alterations [1]. There are two common types of PLLs, integer and fractional – N. Integer PLLs use a Phase and Frequency Detector, a Charge Pump, a Low Pass Filter, a voltage-controlled oscillator and an integer divider, while fractional is using a multi modulus divider and a ΔΣ Modulator (Fig. 1). The role of charge pump is to receive the UP and DOWN signal outputs of the Phase and Frequency Detector and supply or sink current to/from the Low Pass Filter. When the PLL is in lock state, the charge pump does not inject or sink any current.

A charge pump usually presents a non-linear region (Fig. 2) when the phase difference between the input reference clock and the divided clock that enter the Phase and Frequency detector is close to zero. When in lock, a fractional – N PLL with high non-linearity can exhibit noise at the output. In addition, current mismatch is an unwanted effect of a charge pump and it can create high noise and spurious tones because of the ripple it causes to V_{ctrl} (Fig. 3.) [2-4].

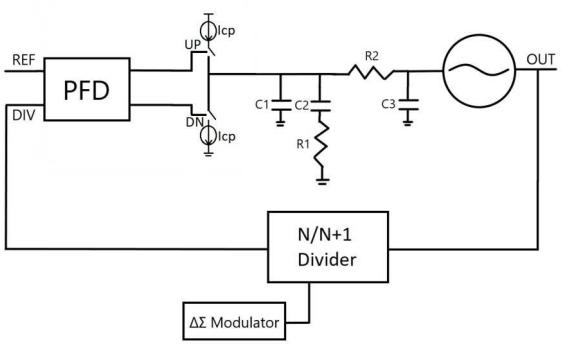

Fig. 1. A fractional - N PLL including a Charge Pump

Furthermore, charge injection is an undesired effect that a charge pump suffers from and can be partially or fully eliminated using different techniques [5]. Finally, channel length modulation cannot be neglected when designing a charge pump because V_{ctrl} can vary from rail to rail. In most common topologies V_{ctrl} is the actual V_{DS} of the nMOS and pMOS transistors that inject or draw current at the output of the charge pump. This current is higher for pMOS when V_{DS} (in this case V_{ctrl}) rises and lower when V_{DS} comes to lower values and can be derived by (1). This phenomenon can affect the overall performance and stability of the phase-locked loop.

$$I_D = \frac{1}{2} K \frac{W}{L} (V_{GS} - V_{th})^2 [1 + \lambda (V_{DS} - V_{DS,SAT})] \quad (1)\ [1]$$

The proposed design offers low power charge pump functionality, dissipating 309uW at 1V combined with very low current mismatch. This charge pump occupies small die area and presents great linearity and low noise. The paper is organized as follows. Section II describes the proposed charge pump design and layout. Section III presents the simulation results of the extracted views and comparisons with other works. Finally, Section IV concludes this work and discuss future improvements.

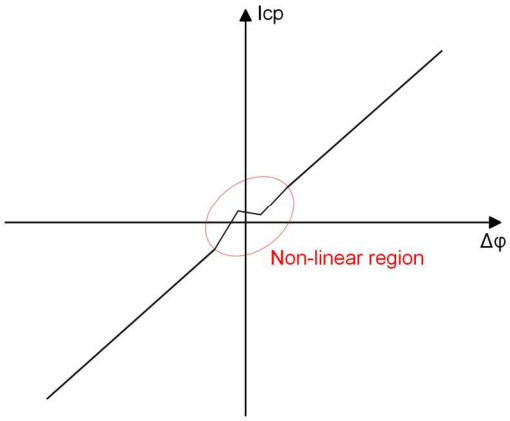

Fig. 2. Non-linear region of a Charge Pump

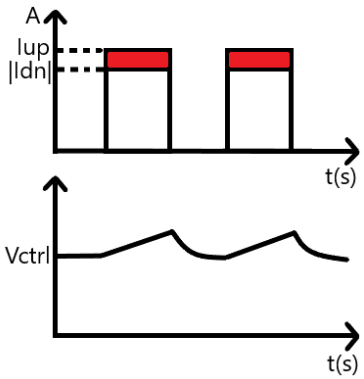

Fig. 3. Current Mismatch can cause ripple to the Vctrl

II. Design of the Proposed Charge Pump Circuit

The signal outputs UP and DN from the PFD are inserted to a single-ended-to-differential circuit which uses a transmission gate as a delay to compensate for the extra inverter in the inverting branch and a latch to ensure the half supply crossing point of the outputs (Fig. 4).

The proposed charge pump design is presented in Fig. 5. In order to eliminate the channel length modulation of P1 and P2, a loop is created, including OA1. This operational amplifier regulates the gate voltage of the transistors P1 and P2 while the V_{out} fluctuates. The output section on the right of Fig. 5 is split into two branches, the actual and the replica. To avoid transient phenomena at the current sources when the UP and DN signals are toggling, transistors P2 and N3 must be in saturation during the whole operation process. Thus, when UP and DN signals are in low logic levels, P2 and N3 transistors will operate and the current will flow through the replica branch. On the other hand, when only UP signal is in logic high level, P2 will inject current to the filter for the first case and at the same time. To keep the current flowing through the N3 transistor, OA2 has been introduced to the circuit and it is connected as a buffer, suppling the current to the N3 transistor when UP is high. On the other hand, when only DN signal is in high logic state, the N3 transistor draws the current from the filter, while the OA2 keeps the current flowing from the P2 transistor. Furthermore, OA2 keeps the middle of the replica branch at the same voltage level as the V_{out}. One more contribution of the active amplifier OA2 is the current mismatch elimination. Due to process variation, transistors P2 and N3 can present a current mismatch. If this happens, OA2 steps in and supplies or draws the necessary current. The OA1 operational amplifier is two-stage with DC gain of 44 dB and GBW of 37MHz and an RC compensation is added as presented in Fig. 5. OA2 is a transconductance amplifier with DC gain of 51 dB and GBW of 31MHz.

To keep the current biasing as uniform as possible, dummy switches are added to the circuit. SW1 and SW2 are always on and recreate the voltage drop of the UP, UPB, DN and DNB switches placed at the actual and the replica branch. Those switches have been designed in order to have the smallest possible voltage drop, which in this case is 15mV. Additionally, MOS capacitors have been added to reduce the charge injection effect [5] as presented in Fig. 6. The switches are complimentary transmission gates and the MOS capacitor values have been selected to match the gate-source parasitic capacitance of the nMOS and pMOS transistors.

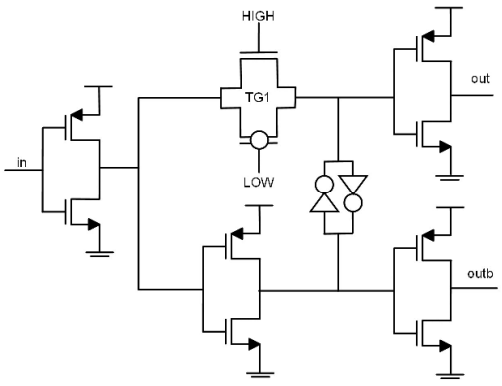

Fig. 4. Single ended to differential clock block

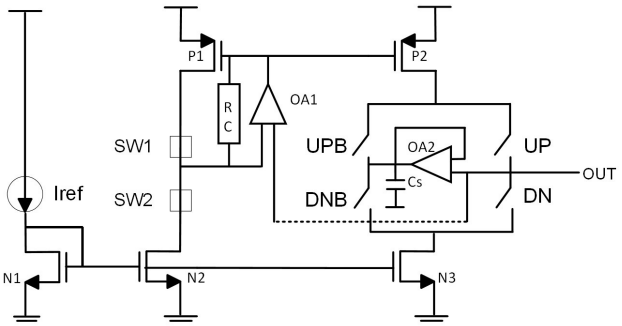

Fig. 5. Proposed charge pump circuit using a smoothing capacitor at the output of the active amplifier

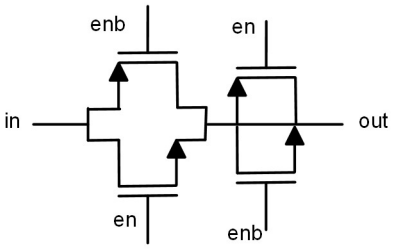

Fig. 6. Complementary switches using MOS capacitors for charge injection reduction

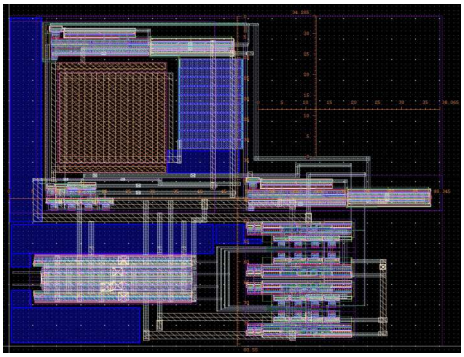

Fig. 7. Top layout of the proposed charge pump

The layout of the proposed design is presented in Fig. 7. Special care has been taken to the symmetry of the differential signals UP/UPB and DN/DNB. Furthermore, wide connections for the current mirror, the replica and actual branch have been implemented. The placement of the switches is in the center of the cell, to ensure the equal distance for each one.

III. Simulation Results

After the extraction of the layout that discussed above, extracted simulations in order to validate the correct functionality and performance took place. All results are simulated using spectre simulator. Typical temperature was set to 60°C to consider the self-heat, slow to -40°C and fast to 125°C. In Fig. 8, the transient outputs for UP/DN and output current is presented at typical. The spikes are kept low enough. In Fig. 9, the linearity over corner is presented. It is obvious that the best performance is for typical, while fast and slow also exhibit good behavior. In Fig. 10, the output currents I_{up} and I_{dn} are presented when sweeping the V_{ctrl}. The useful V_{ctrl} range of this work is from 0.3V to 0.75V. Furthermore, the current mismatch is below 0.01%.

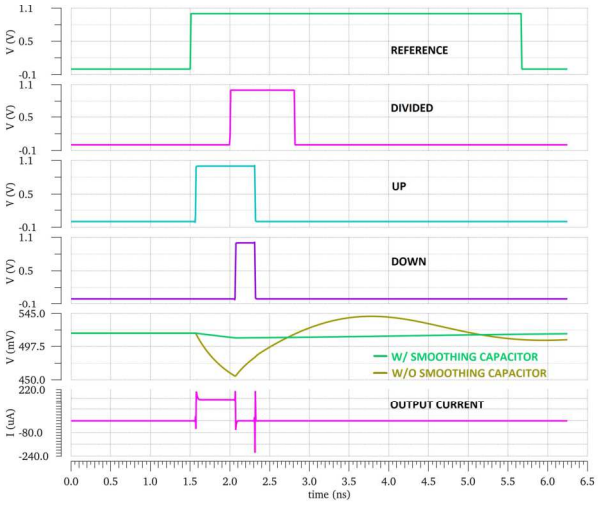

Fig. 8. Transient simulation results

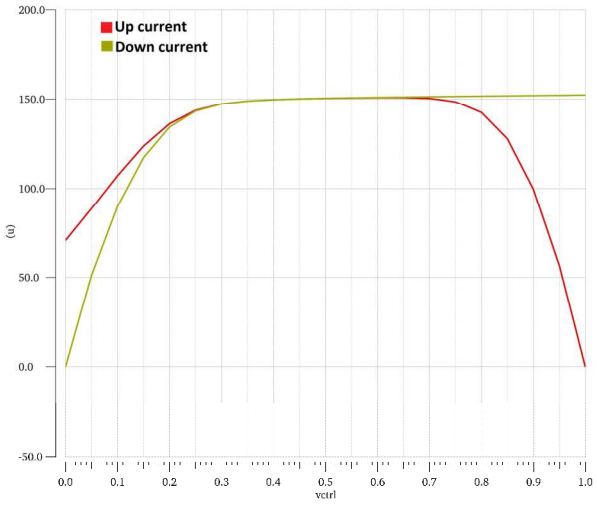

Fig. 10. Vctrl range and current mismatch at the useful area

In Fig. 8, the divided clock is lagging for 500ps and the output current is 150uA. Additionally, the effect of the smoothing capacitor can be seen. The transient phenomenon at the output of the buffer OA2 remains steady and the disruptions that can cause non-linearity are almost eliminated.

In Fig. 9, the output current when the phase difference between the reference and the divided signals is swept between -400ps to 400ps. This range is selected due to the output frequency of the ring oscillator described at [6]. For a fractional – N PLL we presume that due to the ΔΣ Modulator the divided clock will fluctuate between $-4T_{vco}$ and $4T_{vco}$ for a $f_{VCO} = 10\ GHz$.

Additionally, as discussed above, at Fig. 10 the range of the V_{ctrl} and the current mismatch is presented.

Furthermore, a Monte Carlo sweep of the charge pump current for process and mismatch variation is presented at Fig. 11. The mean is 150.107uA and the standard deviation is 1.107uA.

Another result is the output current noise and is presented in Fig. 12. The noise at 1MHz offset is $1.135\ x\ 10^{-24} A^2/Hz$. Moreover, at Fig. 13. the effect of the smoothing capacitor at typical corner is presented. Adding the capacitor, the transient effect at the dummy output is minimized resulting in better linearity performance.

Finally, a table including comparison with other works is presented in Table 1.

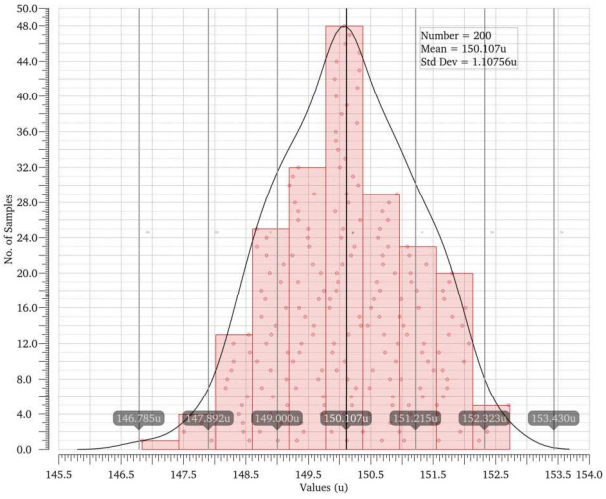

Fig. 11. Monte Carlo simulation of the Charge Pump current

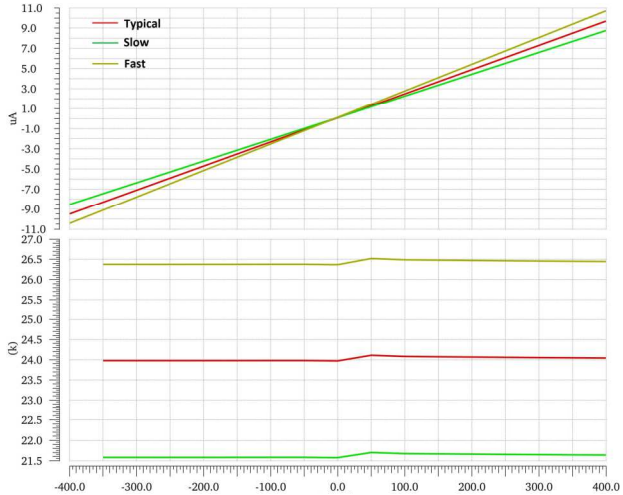

Fig. 9. Output current linearity and the derivative over corners

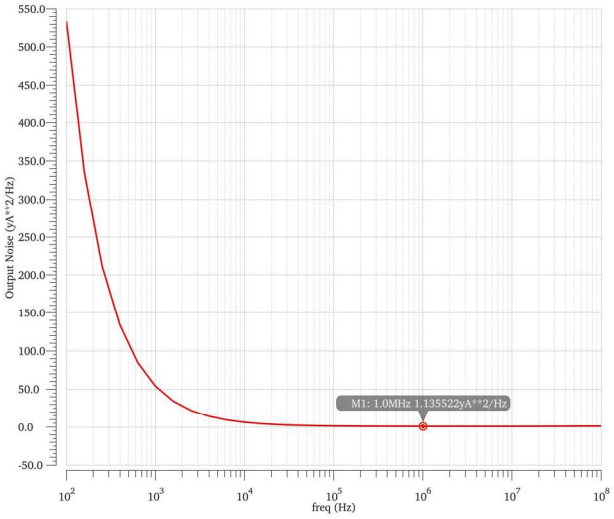

Fig. 12. Output current noise

TABLE I. COMPARISON WITH OTHER WORKS

REF	PERFORMANCE					
	PROCESS	SUPPLY	I_{cp}	$V_{ctrl}\ (V)$	MISMATCH	POWER DISS.
[7]	$90nm$	$1V$	-	$0.5-1$	0.5%	$320uW$
[8]	$55nm$	$1.2V$	$100uA$	$0.2-1$	0.01%	-
[9]	$90nm$	$1.2V$	$100uA$	$0.1-1.1$	0.01%	$1.4mW$
THIS WORK	$65nm$	$1V$	$150uA$	$0.3-0.75$	0.01%	$309uW$

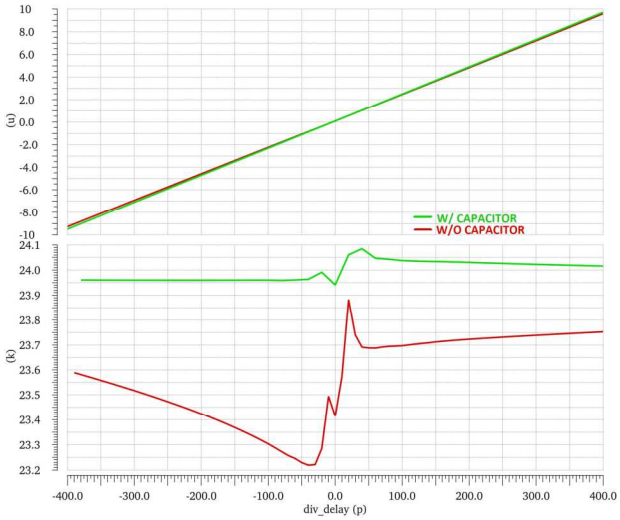

Fig. 13. Comparison of the output current linearity and its derivative with and without the smoothing capacitor

Compared with other works, the proposed design offers low power charge pump functionality, dissipating 309uW at 1V combined with very low current mismatch. Finally, this charge pump occupies small die area and presents great linearity and low noise.

IV. CONCLUSION

In this work, a 65nm charge pump using 1V supply, with a smoothing capacitor, a channel length modulation cancelling operational amplifier and a buffer is presented. According to the extracted results, the V_{ctrl} range is between 0.3 and 0.75V, the current mismatch at the useful range is below 0.01% and the power dissipation is 309uW. The output current noise at 1MHz offset is $1.135\ x\ 10^{-24} A^2/Hz$. The layout requires an area with dimensions of 88um x 80um. Finally, a next step for future work could be a current programmable charge pump for various applications and loop dynamics.

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