A Modified Metal Oxide Memristor Model

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***Abstract* — The memristor is a new and promising electronic memory element and could be a possible replacement for the present CMOS components. Due to its nano size, low energy usage and memory effect, it could be used in neural nets, memory crossbars, reconfigurable analogue and digital devices and other electronic schemes. In this paper, a simple, fast functioning modified metal oxide memristor model is suggested. Its corresponding LTSPICE library model is generated and successfully analyzed in a simple neural network. The model's behavior is in accordance with the basic fingerprints of the memristor elements. Its proper operation and applicability in memristor-based devices is established.**

Keywords—simple memristor model; nonlinear ionic drift; metal oxides; LTSPICE memristor library model; neural network

I. INTRODUCTION

The resistance switching behavior in transition metal's oxide materials has been analyzed since 1970 [1], [2]. These effects are related to the change of the oxide material resistance in accordance with both the applied voltage signal and the accumulated electric charge [2]. These oxide materials could hold their conductance and state for a long-time interval after switching the electric sources off [3]. They store electric charge corresponding to the time integral of the voltage signal [4]. From this point of view, transition metal oxides as TiO_2, HfO_2, Ta_2O_5 and others could be used as storing elements in memory schemes [1], [4]. In 1971 Chua has predicted the fourth basic two-terminal passive nonlinear element – the memristor [3]. In 2008 the first physical prototype of memristor based on TiO_2 is generated by Hewlett-Packard research group guided by Williams [4]. After this important invention, many scientific teams tried to create memristors, applying different technologies and materials. Several different type memristor elements, made of polymeric compounds [5], spin magnetic systems [6], amorphous silicon dioxide [7] and others are reported in the scientific literature [8]. Several of the main advantageous memristor properties are their non-volatility, memory effect, low energy usage, high switching rate, sound compatibility to the present CMOS integrated circuits technologies, and nano-scale size [4], [8]. These useful properties are related to their potential applications in non-volatile memory schemes, reconfigurable digital and analogue circuits, neural networks and other electronic devices [8], [9]. The engineering of electronic schemes requires their preliminary analysis by computer simulations [10], [11]. LTSPICE is a very appropriate environment for such investigations because it is a user-friendly, simple and free software [11]. Several specific models for TiO_2, $1HfO_2$, and Ta_2O_5 memristors are existing in the technical literature [12], [13]. Owing to several specific aspects of their structure, principles of operation and behavior in electric field, these memristor elements are considerably different [13]. Nevertheless, in some cases general models could be used for a large class of transition metal oxide-based memristor elements. In many cases, the specific models for metal oxide memristors are quite complex [12], [14]. The main goal of this paper is to suggest a simple, fast-operating and general LTSPICE memristor model, appropriate for analysis and simulations of a broad class metal-oxide based memristors [12], [15]. The considered simplified memristor model is mainly founded on both the Lehtonen-Laiho model [14] and the Biolek window function [16]. Its main advantages, with respect to the existing models, are the simple realization and the fast functioning. Another advantage of the offered memristor model is the inclusion of activation (sensitivity) thresholds, which ensure its usage in artificial neural nets and memory matrices [17], [18], [19]. The proposed model is successfully applied in a simple neural network for XOR logical function representation [20], [21], [22]. After comparison to experimental current-voltage relations [4], [15] and to the results obtained by several of the frequently used memristor models [17], [18], [22], [23], it is established that the proposed model has a comparatively good precision. For restriction of the state variable and expression the boundary effects for hard-switching operation, a modified Biolek window function [23], [24] is used. For prevention of convergence issues an enhanced and differentiable step-like sigmoidal function is used in the correspondent LTSPICE memristor library model.

The rest of the paper is constructed as follows. Section 2 presents a short description of the transition metal oxide memristors and their models. The suggested general memristor model is expressed in Section 3. The respective LTSPICE realization of the memristor model is presented in Section 4. Its application in a simple neural network is discussed in Section 5. Section 6 concludes the paper.

II. AN OVERVIEW ON METALOXIDE-BASED MEMRISTORS

For better introduction and understanding of the memristor operation and their modeling, a brief explanation of the fundamentals of metal-oxide based memory components is first presented. The respective state variable for TiO_2 and HfO_2-based memristors is presented as a ratio between the lengths of the doped layer w and of those of the whole memristor element D [4]. For tantalum oxide-based memristors the state variable is expressed as a ratio between the surfaces of the central conduction region a_1 and those of the whole memristor cross-section a_2 [13]. The state variable x then could be described by (1) [4], [13], [18]:

$$x = \frac{w}{D} = \frac{a_1}{a_2},\ 0 \le x \le 1 \tag{1}$$

The state-dependent relation between the applied memristor voltage signal v and the respective current i flowing through the memristive element is [4], [18]:

$$v = M(x) \cdot i = \left[R_{ON} x + R_{OFF} (1 - x) \right] \cdot i \tag{2}$$

The author/s would like to thank the Research and Development Sector at the Technical University of Sofia for the financial support.

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where (2) is related to Strukov-Williams memristor model [4], R_{ON} and R_{OFF} are the ON-state and OFF-state resistances and $M(x)$ is the state-dependent resistance of the memristor element, known as a memristance [18]. The equations fully describing a memristor element contain the state expression, relating the time derivative of the state variable x and current, and the state-dependent current-voltage relationship [18]:

$$\begin{vmatrix} x'_t = k \cdot i \cdot f(x,i) \\ v = i \cdot M(x) \end{vmatrix} \quad (3)$$

where $f(x,i)$ in the general case is a window function, used for restriction of the state variable x in the range (0,1) and for expression of the related boundary effects, and k is a coefficient, dependent on the physical properties of the memristor – the ionic drift mobility μ, the ON-state resistance R_{ON} and the memristor element's length D [4], [24]:

$$k(v) = \mu(v) \cdot R_{ON} \cdot D^{-2} \quad (4)$$

The ionic dopant drift mobility μ depends on the memristor voltage. It rises exponentially when the electric field intensity goes beyond a threshold value [24]. The associated physical processes are very complex and could not be precisely expressed by a simplified model. The commonly used Lehtonen-Laiho memristor model is a precise one and is expressed by the next equations' set [14]:

$$\begin{vmatrix} i = x^n \cdot \beta \cdot \sinh(\alpha v) + \chi\left[\exp(\gamma v) - 1\right] \\ x'_t = a \cdot v^m \cdot f(x,i) \end{vmatrix} \quad (5)$$

where β, α, χ, γ, a, m, and n are parameters for adjustment of the model [14]. The first term in (5) represents the state-dependent current, while the second one expresses its exponential increase with the voltage [14]. In order to simplify the memristor model, an approximate representation of the exponential ionic dopant drift is expressed in the next section.

III. The Proposed General Memristor Model

The suggested modified memristor model is expressed by (6). Here, the coefficients k_1, k_2, k_3 and k_4 are tuning parameters. The first equation is a fragment of the Lehtonen-Laiho model [14] and presents the relationship between the memristor voltage v and the current i. For simplification of the proposed model, the second exponential term in the original Lehtonen-Laiho model (5) is ignored. The second equation in (6) presents the time derivative of the state variable x as a function of the memristor voltage and current.

$$\begin{vmatrix} i = k_1 x^3 \cdot \sinh(k_2 v) \\ x'_t = \left[k_3 v \cdot \exp(k_4 v) \cdot f_{BM}(x,i)\right] \cdot stpp(v - v_{thr}) \end{vmatrix} \quad (6)$$

The step-like function stpp(.) is represented in (7). It is a differentiable and flat version of the standard Heaviside function. Its inclusion leads to a slow transition between the states of the memristor for voltages, lower or higher than the activation threshold v_{thr} and to a partial avoidance of convergence problems in SPICE environment. The included in (6) modified Biolek window function $f_{BM}(x,i)$ together with the smooth function $stpp(i)$ are presented by (7) [16], [23]:

$$\begin{aligned} stpp(v) &= \frac{1}{2} \cdot \left[v\left(v^2 + s\right)^{-0.5} + 1 \right] \\ f_{BM}(x,i) &= 1 - \left[x - stpp(-i) \right]^{2p} \end{aligned} \quad (7)$$

The parameter s included in the final equation determines the sharpness of the sigmoidal function around the switching point. It frequently has a value in the range between 0.001 and 0.00001 [11], [23]. When the absolute value of the voltage signal's level is lower than the sensitivity threshold v_{thr}, then the memristive element behaves as a simple resistor and the correspondent time derivative of x is zero [9], [17]. If the memristor voltage is higher than the activation threshold v_{thr}, then the alteration of the state variable x is proportional to the memristor voltage. The exponential term $exp(k_4 v)$ is applied to approximate representation of the nonlinear ionic dopant drift [24]. The suggested memristor model is analyzed for sinusoidal signals in both soft-switching and hard-switching operating modes. The optimal values of the proposed memristor model's parameters are obtained applying a technique for parameter estimation, based on simulated annealing and gradient descent of the root mean square error between the experimental and the simulated memristor current [18]. The simulation time of the proposed model is about 17.61 ms, for Lehtonen-Laiho model - 19.34 ms, for Joglekar model – 16.17 ms, and for Biolek's model – 16.45 ms. The corresponding errors are: about 2.75 % for the offered model, 2.62 % for Lehtonen-Laiho model, 5.43 % for Joglekar and 3.88 % for Biolek's model. The optimal values of the model's parameters are: k_1=0.0024, k_2=2.5981, k_3=568.86, k_4=0.6469, p=20, v_{thr}=0.1 V, x_0=0.6367. The time graphs of the memristor voltage, current and state, and the related current-voltage relationships are shown in Fig. 1 for comparison the characteristics and confirmation of the its correct operation.

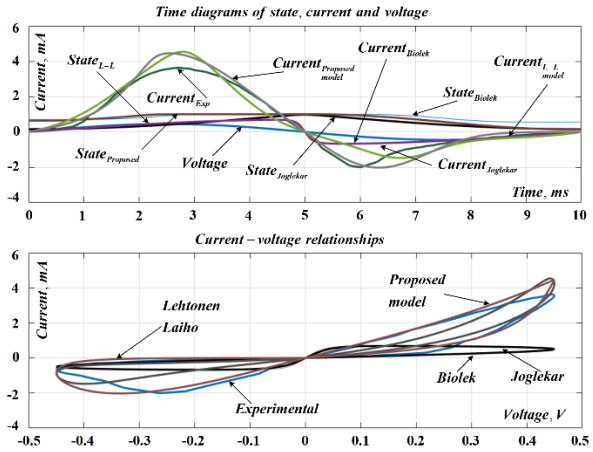

Fig. 1 Time diagrams of the memristor voltage, experimental and simulated current and the correspondent current-voltage relationships, according to the proposed model, Biolek, Joglekar and Lehtonen-Laiho memristor models

Dynamic root maps (DRM) express the dependence between the state and its time derivative in a state space. They are frequently used for comparison the behavior of memristor models [25]. The DRM of the proposed model and Lehtonen-Laiho models have similar representations. Using (6) and (7), LTSPICE model is generated and described in next section.

IV. LTSPICE Realization of the Memristor Model

Founded on the suggested modified memristor model, expressed by (6) and (7), a corresponding LTSPICE [11], [23] model of the considered metal oxide-based memristor component is generated. The main functional modules in the LTSPICE software [11] are used for the respective mathematical operations, according to the discussed memristor model. The equivalent schematic of the created LTSPICE memristor model is presented in Fig. 2 for additional explanations and discussion.

The memristor state variable x is proportional to the voltage $V(Y)$ across the capacitor C_1 [23]. Its current is proportional to the time derivative of the state variable x. The two-terminal voltage-dependent current source G_1 expresses the conductance of the oxide memristor component. The resistance of the used voltage source V_1 is expressed by the resistor R_1. These two elements are not included in the LTSPICE code. The resistor R_2, which is connected in parallel to the capacitor C_1 protects the circuit from convergence problems [11], [23]. The basic terminals of the element are the anode (a) and the cathode (c). The terminal Y is optional and is used for observation of x.

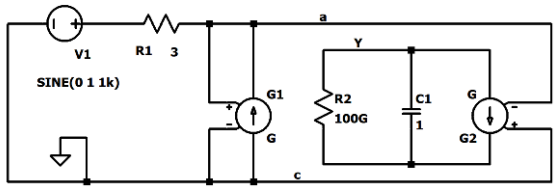

Fig. 2 A schematic of the equivalent LTSPICE memristor model

According to the presented schematic, the respective LTSPICE code of the memristor element is generated. The coefficient m controls the acuity of the step-like function *stpp*.

```
.subckt A12 a c Y
.params k1=0.0024 k2=2.5981 k3=568.86 k4=0.6469
.params C1=1 pp=20 m=1.2337.10-4 vthr=0.1
Cint Y 0 1 IC=0.6367
R2 Y 0 100G
G2 0 Y value={(k3*V(a,c)*exp(k4*V(a,c))*
(1-pow((V(Y)-stpp(-I(a),m)),(2*pp))))*
(stpp((abs(V(a,c))-vthr),m))}
G1 a c value={k1*pow(V(Y),3)*sinh(k2*V(a,c))}
.func stpp(x,p)={0.5*(1+(x/sqrt(pow(x,2)+p)))}
.ends A12
```

The generated LTSPICE memristor model is analyzed by sinusoidal voltage signals with different frequencies. The correspondent current-voltage relationships are presented in Fig. 3 for expression of the proper operation of the memristor model. It is visible that, when the frequency of the voltage signal increases, then the surface of the pinched current-voltage hysteresis loop decreases. This is in accordance with the fundamental fingerprints of the memristors [8], [18]. The model is also analyzed at pulse mode, representing soft-switching and hard-switching operation. According to the original Lehtonen-Laiho model [14], the proposed model is with a higher operating rate. The accuracy of the suggested model is very near to the Lehtonen-Laiho model, according to the obtained root mean square errors.

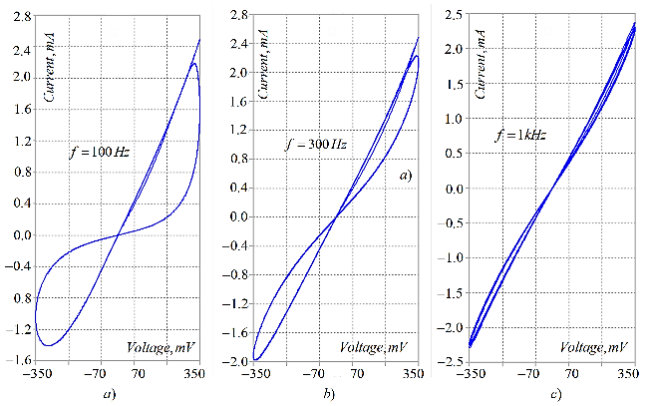

Fig. 3 Current-voltage relationships of the memristor model for different frequencies a) f = 100 Hz; b) f = 300 Hz; c) f = 1 kHz

V. Application in a Simple Neural Network

A simple feed-forward neural net for XOR (eXclusive OR) function representation [20], [21], [22] is shown in Fig. 4 for a detailed description of its functioning and structure. Supervised learning is used for tuning the weights of the synapses, which are based on memristor elements. The other components of the net are founded on CMOS components. The input logical signals are combined with white Gaussian noise. The neural net has two inputs, used for the logical signals x_1 and x_2. It has two hidden layers and an output layer. The neurons in the hidden layers have tangent sigmoidal activation function, while the neuron in the output layer is with a linear one. The first hidden layer of the network contains four neurons. The second hidden layer has three neurons [22]. The output layer contains one neuron.

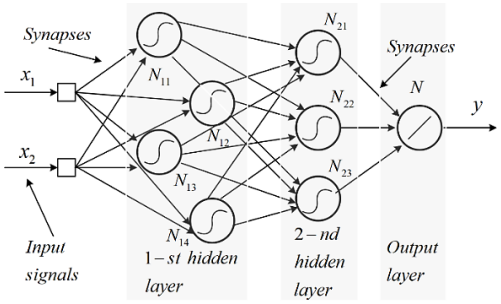

Fig. 4 A schematic of a simple neural network for XOR representation

The time diagrams of the input signals x_1 and x_2 for testing the neural network are shown in Fig. 5 for visual expression of the logical signals. These signals correspond to logical zeros and ones for the emulation of XOR operation. The signals for training the neural network are similar, but they are shifted with respect to the signals for testing, and in this way more realistic results are obtained. The desired signal and the output signal after testing the neural net are presented in the same figure for confirmation of their very good coincidence. The error signal is expressed as a difference between the output signal and the desired signal. The amplitude of the error signal is about ten thousand times lower than the input logical signals' levels. The correct operation of the neural network and the sufficient convergence of the training procedure are confirmed by the obtained results.

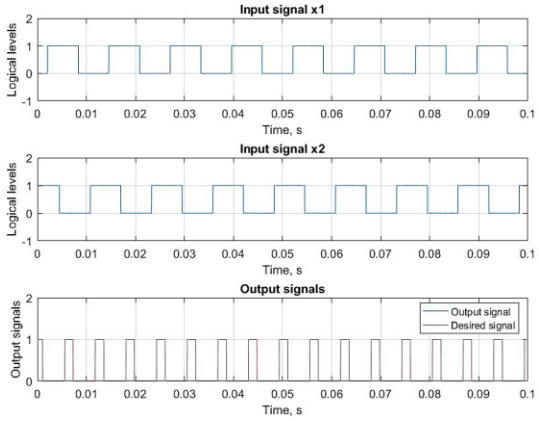

Fig. 5 Time diagrams of the input logical signals x_1 and x_2, the desired and the actual output signals of the neural network during the testing procedure

The schematic of the memristive synapse is shown in Fig. 6 for description of its operation. It includes a memristor M, three resistors R_1, R_2 and R_3 and an amplifier. The current

divider contains two branches. The first branch includes a memristive component M and a resistor – R_3. The next branch has the resistors R_1 and R_2, connected in a series. The currents flowing through these branches are denoted by i_1 and i_2, respectively. The input voltage is v_{in}. The weight of the considered synaptic circuit w as a function of M is [22]:

$$w(M) = \frac{v_{out}}{v_{in}} = k_v \left(\frac{R_2}{R_1 + R_2} - \frac{R_3}{M + R_3} \right) \quad (8)$$

The resistance of the memristor M and the respective synaptic weight w are changed by external voltage impulses. After a simple conversion of (8) and having in mind that $R_2 = R_3$, it is derived that if $R_1 = M$, then $w = 0$. Positive weights are obtained when $M > R_1$. If $M < R_1$ then $w < 0$. Scaling of synaptic weights is realized by altering the voltage transfer coefficient k_v of the applied operational amplifier.

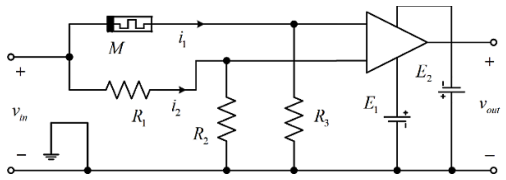

Fig. 6 A schematic of the applied memristor-based synapse

The time diagrams of the input voltage of the synapse and its weight update are presented in Fig. 7 for description of its tuning process. The input signal is a sequence of positive and negative pulse packages. An impulse with a duration of 1 μs and a level of 1 V causes the change of the weight by 0.23 Positive polarity voltage is used for decreasing the weight.

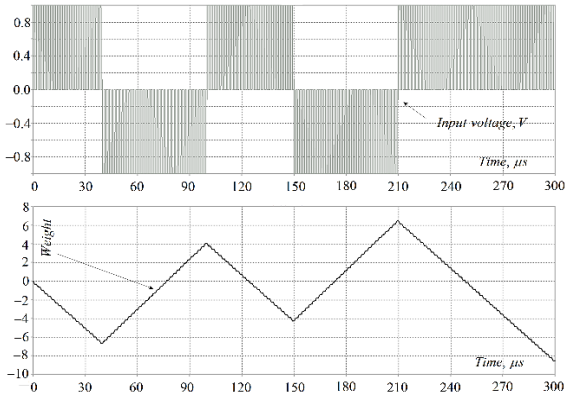

Fig. 7 Time diagrams of the input voltage of the synapse and the correspondent change of the synaptic weight

VI. Conclusion

In this paper, an enhanced and simplified model for transition metal oxide memristor is presented. It is based on the Lehtonen-Laiho and Biolek models and has their main advantages – comparatively high accuracy and proper representation of the boundary effects. The proposed memristor model is applied to a simple neural network for XOR function emulation, which uses memristor-based synapses. The used synaptic circuit is based on a current divider and operational amplifier. The functioning of the applied synaptic device is based on comparison of the currents through the memristive element and a resistor. A benefit of the applied circuit is its ability to produce positive, zero and negative weights. The synaptic circuit one memristor per synapse, which is it's another advantage, rendering to several existing synaptic schemes. The considered memristor model operates in neural networks and it is appropriate for analysis of complex schemes.

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