System-level model of a two-step locking technique applied in an all-digital Phase-locked loop

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***Abstract*—This paper proposes a system-level model of a new two-step locking technique for an all-digital phase-locked loop (ADPLL). The proposed design provides solutions for the trade-offs between the frequency resolution and locking range as well as between design complexity, area, and power consumption of the ADPLL system. As example, a system with reference frequency of 125 MHz and a locking frequency range from 5.375 GHz to 6.25 GHz is designed. The simulated phase-noise performance is -95 dBc/Hz at 1.25 MHz offset employing a division factor between 43 and 50.**

***Index Terms*—All-digital PLL (ADPLL), Time-to-digital converter (TDC), frequency generation, Simulink, MATLAB, Phase noise**

I. Introduction

In recent years, phase-locked loops (PLLs) are widely used in communication applications like synthesiser and clock generator. Various architectures of PLL are designed for different requirements. Some industry demanded requirements are small-area and low-power consumption. Analogue charge-pump PLLs provide better phase noise performance than digital PLLs [1]. However, analogue PLLs occupy more chip area. While the digital PLL meets the above mentioned industry demands, it is also more robust against PVT variations. Also, analogue blocks need a complete redesign when ported to a new technology, thereby increasing the design time. Although, reducing the number of analogue blocks in the mixed-signal ICs can reduce the design cycle, digital PLLs are easily scalable and portable. Hence, ADPLLs are widely preferred [2] - [3].

A conventional time-to-digital based ADPLL suffers from the trade-off between the frequency resolution and the frequency range. To achieve a wider frequency range, the resolution of the time-to-digital conversion (TDC) needs to be decreased, which degrades the in-band phase noise performance of the system. Based on

$$S_{TDC} = \frac{(2\Delta_{TDC} f_{out})^2}{3 f_{ref}}, \tag{1}$$

in order to achieve a phase noise of $-100\,\mathrm{dBc/Hz}$, the resolution of the TDC should be at least $10\,\mathrm{ps}$ [4].

For higher frequency resolution, the frequency range of the system is limited. And for higher resolution, more delay stages are needed and hence the area and the power consumption of the system increases. To overcome these problems, a solution is proposed, in which the ADPLL locks with two stages: coarse and fine locking. The coarse locking uses a simple frequency error averaging technique [5] and the fine locking uses two TDCs along with the delta-sigma modulator and a digital-loop filter, which filters the output of the system. With the high resolution TDC and a delta-sigma modulator with digital-loop filter, a better in-band phase noise can be achieved.

II. The proposed ADPLL

The proposed architecture of the all-digital PLL is shown in Fig. 1. During *RESET*, the coarse control block is set with a initial value. When the *RESET* signal is set low, the fine-locking stage is disabled and the digitally-controlled oscillator (DCO) starts operating at a given frequency set by the initial value. The output of the DCO is then divided by the frequency divider, by a factor of *N*, and the divided output clock, CLK_{DIV} is given to the phase frequency detector (PFD). The PFD detects the phase difference between the CLK_{REF} and CLK_{DIV}, and gives the *SIGN* signal which gives the information of whether CLK_{DIV} signal is leading or lagging. The *SIGN* signal is used for the coarse locking of the PLL. Based on the *SIGN* signal, the coarse control block either increases or decreases the frequency of the DCO and calculates the frequency difference between the current frequency and the target frequency. Once the DCO locks at a frequency, coarse locking is achieved and the fine locking process begins. During fine locking, the offset information from the PFD is given to the TDC block. The TDC block consists of two types of TDCs which are the delay-line-based and the Vernier-type TDC. The output of the delay-line-based TDC is encoded and given to the integrator which tunes the DCO accordingly. The output of the Vernier-type TDC is encoded and given to the delta-sigma modulator through a DLF, which filters the noise and tunes the DCO in the kilohertz range.

A. Phase Frequency Detector

The PFD block generates *START*, *STOP*, and *SIGN* signal as illustrated in Fig. 2. The *UP* and *DOWN* signals are pulled up to logic 1 when CLK_{REF} and CLK_{DIV} trigger two D-flip flops (DFFs). If CLK_{REF} leads CLK_{DIV}, the *UP* signal goes to logic HIGH when CLK_{REF} triggers followed by the *DOWN* signal when CLK_{DIV} triggers. When CLK_{DIV} leads CLK_{REF}, then the *DOWN* signal goes to logic HIGH first, followed by the *UP* signal. When both *UP* and *DOWN* are logic HIGH, the flip flops, DFF_2 and DFF_3, reset. The time difference between the *UP* and the *DOWN* signals going to logic HIGH is the phase

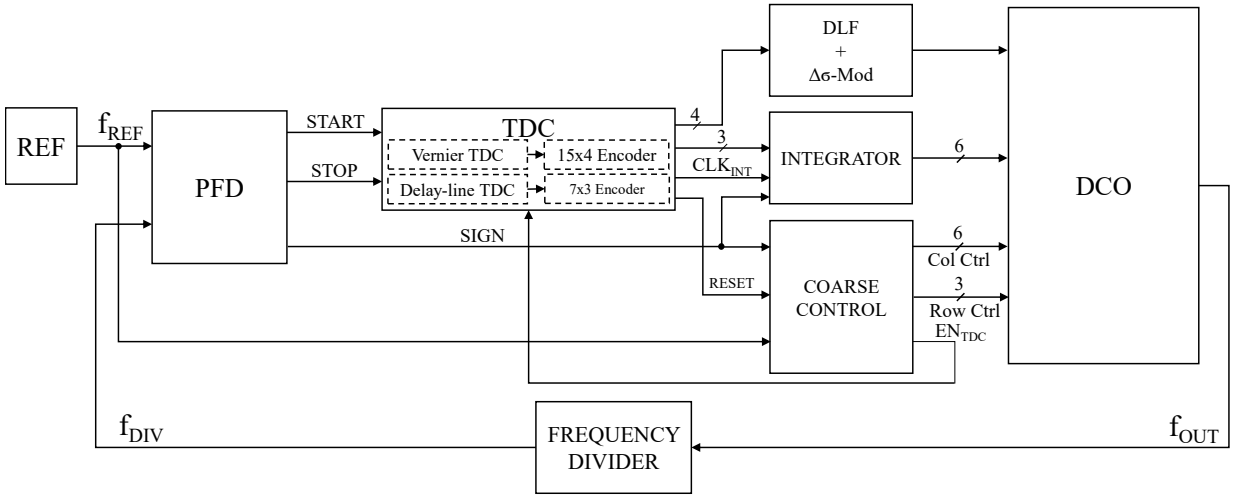

Fig. 1: Block diagram of the proposed ADPLL.

difference between the CLK_{REF} and CLK_{DIV} signals. *START* and *STOP* signal is the logic OR and logic AND of the *UP* and *DOWN* signals. The *SIGN* signal is generated via DFF_1. The SIGN signal is logic HIGH when CLK_{REF} leads CLK_{DIV} and logic LOW when CLK_{DIV} leads CLK_{REF}.

B. Time-to-Digital Converter

The delay-line based TDC has a single inverter-based delay line. Each inverter stage has a delay time of 176 ps. The *START* signal from the PFD is delayed along the delay-line and is given to the input of the flip-flops. The *STOP* signal is given directly to the clock of the flip-flop, which triggers the output of the flip-flops. The delay stages which already passed the flip-flops give a HIGH value at the output, and all other stages give a LOW value. Each HIGH value corresponds to the time interval between *START* and *STOP* signal. The output of this TDC is encoded with a 7x3 encoder and given to the integrator as shown in Fig. 1. A Vernier-type TDC consists of two delay lines: one for the *START* and one for the *STOP* signal. The

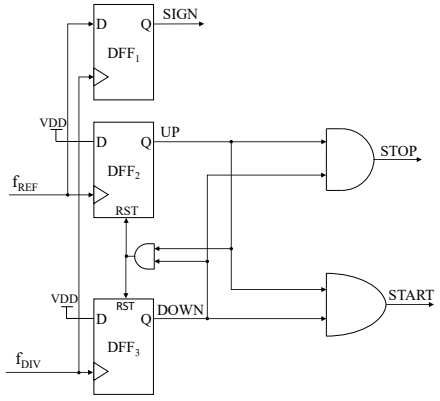

Fig. 2: Block diagram of a phase frequency detector.

delay elements for the *START* signal, t_{START} are marginally larger than the delay elements for the *STOP* signal, t_{STOP}. The resolution of the Vernier-type TDC is the difference between t_{START} and t_{STOP}. The *START* delay line is used as the input whereas the *STOP* delay line is fed to the clock of the flip-flops. The *START* signal occurs first and sees a larger delay through the delay line than the *STOP* signal which occurs later. Hence, the *STOP* signal races against the *START* signal. The delay time is determined with the help of the flip-flops when both *START* and *STOP* signals are in-phase. The output of a stage is HIGH, if the *START* signal occurs first. For all following stages, *STOP* signal occurs first resulting in a logic LOW state at the output. The output of the Vernier-type TDC is given to the 15x4 encoder and passing on to the low-pass filter and to the delta-sigma modulator. The clock signal for the integrator, CLK_{INT} is the delayed *STOP* signal in the slow delay line from the Vernier-type TDC.

C. Coarse Locking

The architecture for the coarse control block is shown in Fig. 3. In *RESET*, the counter is set to an initial value and the EN_{TDC} signal is kept at logic zero. So, the counter value is sent to the row and column control. The counter is enabled by the inversion of the EN_{TDC} signal and the CLK_{REF_delay} is the delayed version of the reference signal, CLK_{REF}. For every clock the bidirectional counter counts up or down based on the *SIGN* signal. The output of the counter is given to the multiplexer (MUX) and to the register blocks. When the *SIGN* toggles, the register clock block generates the CLK_{MAX} or CLK_{MIN} output signals. These clock signals are generated only during the coarse locking. Based on these clock signals, the register block stores the last 2 maximum and minimum counter value to the MAX or MIN registers. The CONTROL CHECK block checks if these values are within a set tolerance. If so, EN_{TDC} signal is set and also the average value of the maximum and minimum values is computed. This average value is set to the row and column control blocks via the

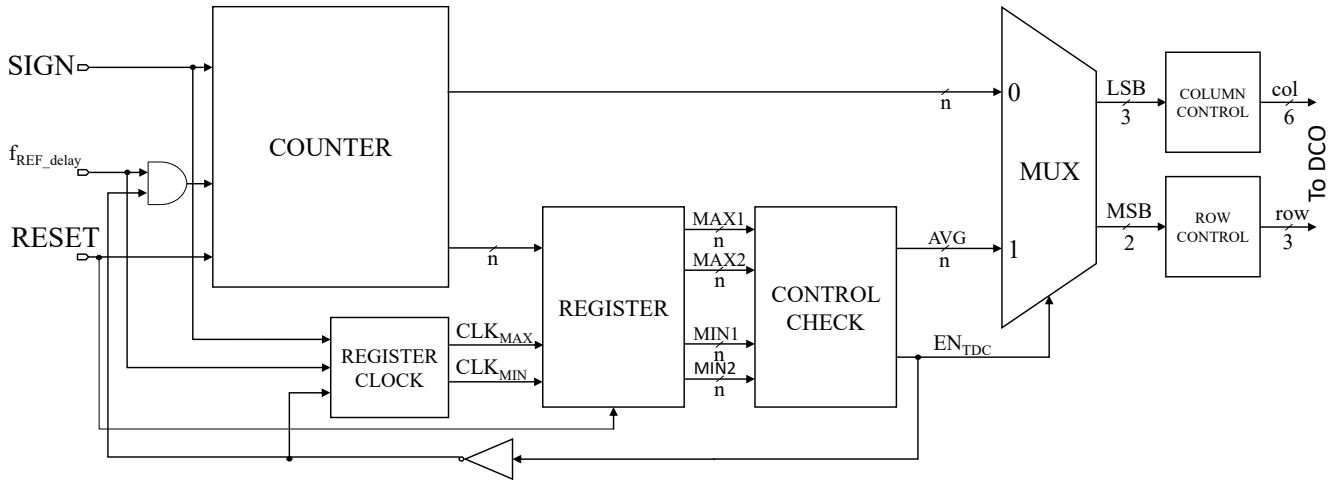

Fig. 3: Block diagram of the implemented coarse control architecture.

MUX. The EN_{TDC} signal disables the counter and also enables the fine locking. The row and column control blocks are 2-to-3 converters and 3-to-6 converters. The coarse locking stage tunes the DCO in the gigahertz range.

D. Fine Locking

The fine locking of the proposed architecture is done in 2 stages. The first stage locks with the integrator block and the second stage uses the low-pass filter with the delta-sigma modulator. The integrator takes its input from the delay-line-based TDC and adds or subtracts it from its previous value based on the *SIGN* signal. The output of the integrator is given directly to the DCO and its frequency is tuned in the megahertz range. The outputs of the Vernier-type TDC is given to the delta-sigma modulator via the DLF. This stage helps in filtering the noise and to achieve better phase-noise performance by pushing away the phase noise from the band of interest. The DCO is thus tuned in terms of kilohertz. The digital loop filter and the delta-sigma modulator are not implemented in Simulink as the Simulink does not support the high resolution needed in time-domain simulations. The phase noise of the system is calculated by using (1) and

$$S_{REF}(f) = k_0 + \frac{k_1}{f} + \frac{k_2}{f^2} + \frac{k_3}{f^3}, \tag{2}$$

$$S_{DCO}(f) = k_0 + \frac{k_2}{f^2} + \frac{k_3}{f^3}, \tag{3}$$

$$S_{DSM} = \frac{\pi[2\sin(\frac{\pi f_{out}}{f_{S\Delta}})]^{2(m-1)}}{3f_{S\Delta}}, \tag{4}$$

where k_0 represents the thermal noise, $\frac{k_1}{f}$ represents the flicker noise, $\frac{k_2}{f^2}$ represents the carrier noise, $\frac{k_3}{f^3}$ represents the inter-modulation of both carrier and transistor noise, $f_{S\Delta}$ and m represent the sampling frequency and the order of the delta sigma modulator, f_{out} is the output frequency of the ADPLL, and f_{ref} is the frequency of the reference signal [4].

E. Digitally-Controlled Oscillator

The DCO is designed by using a user-defined block in simulink. A matlab code is added into the simulink block to control the output frequency. The block gets its inputs from the coarse control block, integrator block, and the delta-sigma modulator. Based on its inputs, the block looks for it corresponding frequency in the lookup table and oscillates at that frequency. The frequency of oscillation updates as soon as any of its input toggles. The frequency range for the coarse locking stage is between $5.252\,\text{GHz}$ and $6.344\,\text{GHz}$ with an average frequency step of $40\,\text{MHz}$. For fine locking with the integrator block, the frequency increases in steps of $1\,\text{MHz}$.

III. Simulation Results

The transient simulation of the proposed ADPLL system is shown in Fig. 4. While the reference signal of CLF_{REF} is equal to $125\,\text{MHz}$, the output of the DCO, CLK_{OUT} is equal to $6\,\text{GHz}$. When coarse locking is enabled, for every rising and falling edge of the *SIGN* signal, the maximum and minimum values by the counter are stored in the registers. As observed in Fig. 4, after storing two maximum and minimum values, the coarse locking stage computes the average value and enables the fine locking. The toggles in the *SIGN* signal after coarse locking shows the working of the integrator block for fine locking. Fig. 5 shows the output of the coarse locking stage with the *SIGN* signal. The two minimum ($MIN_{1,2}$) and maximum values ($MAX_{1,2}$) stored in the register are 15, 16, 23, and 22, respectively. Since, the two maximum and minimum values in the register are close enough, the average value can be computed. The computed average value is equal to 19. The phase-noise plot of the system is shown in Fig. 6. It is plotted by using (1)-(4), with f_{ref}, f_{out}, $f_{S\Delta}$, and Δ_{TDC} as $125\,\text{MHz}$, $6\,\text{GHz}$, $1\,\text{GHz}$, and $11\,\text{ps}$, respectively. The loop bandwidth of

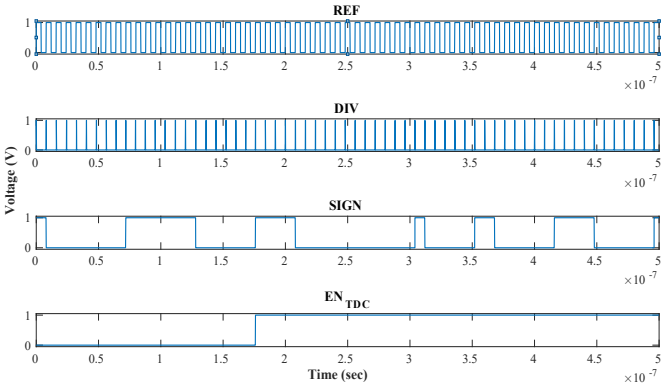

Fig. 4: Transient simulation of the coarse part of the proposed ADPLL.

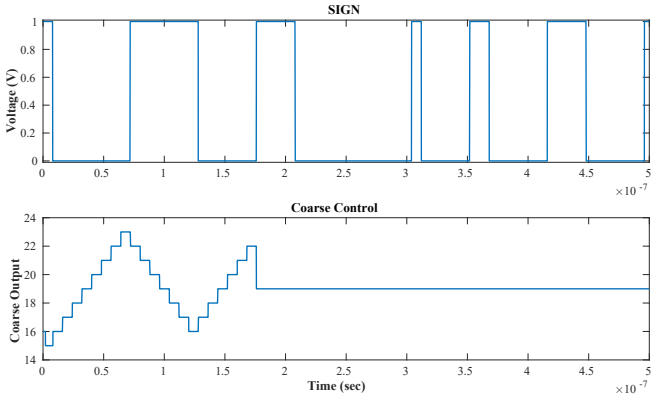

Fig. 5: Output of the coarse control with *SIGN*.

the system is equal to $1.5\,\mathrm{MHz}$. As illustrated in Fig. 6, the in-band phase noise is dominated by the reference signal and the TDC, while the loop bandwidth is small enough to suppress the TDC noise and large enough to suppress the DCO noise.

IV. Conclusion

A new two-step approach locking technique of the ADPLL is introduced. Coarse locking with averaging technique has been simulated and verified with MATLAB Simulink.

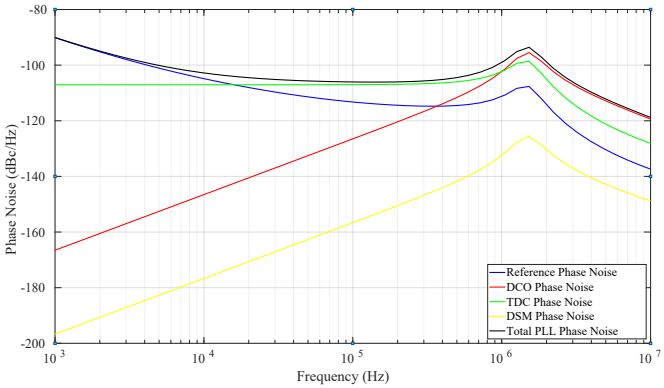

Fig. 6: Phase-noise simulation of the proposed ADPLL.

The generated output clock operates between $5.252\,\mathrm{GHz}$ and $6.344\,\mathrm{GHz}$. The coarse locking architecture averages the frequency based on the maximum and minimum values stored in the registers. The proposed ADPLL achieves thus a wide tuning range with the coarse locking architecture and kilohertz range resolution with the fine locking architecture. The trade-off between the resolution of the TDC, resulting in high phase-noise performance, and wide locking range which requires wide range of TDC can be alleviated through the implemented architecture. In this way, small occupied area and low power consumption are achieved by keeping the TDC small without sacrificing the locking range of the ADPLL. The simulated phase noise of the proposed ADPLL with a TDC resolution of $11\,\mathrm{ps}$ is $-95\,\mathrm{dBc/Hz}$ at $1\,\mathrm{MHz}$ offset.

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