Realization of Memristor-aided Logic Gates with Analog Memristive Devices

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***Abstract*—Computation based on the von Neumann architecture suffers from the data transfer between computation unit and memory, i.e. the so-called von-Neumann bottleneck. Thus, new computing paradigms emerge leveraging in-memory computing (IMC). Stateful memristor aided logic (MAGIC), which has attracted great attention in recent years, enables the realization of a functionally complete set of Boolean logic functions within a memristive memory array. Whereas typically digital-switching memristive devices are exploited, in this work, we investigate the realization of MAGIC gates using analog-switching $BiFeO_3$ (BFO) devices. The simulation results reveal that the MAGIC NIMP gates, as proposed for a digital-switching memristive device, do not work correctly with the analog BFO devices. By studying the input drift and blocking effect while operating MAGIC NIMP gate, we propose two alternative MAGIC gates by exploiting analog memristors, i.e. a NOR gate and a -P gate.**

***Index Terms*—memristor-aided logic, analog memristor, switching dynamics, current blocking effect, input drifting**

I. Introduction

Traditional computation systems are based on the von-Neumann architecture [1]. In the von-Neumann architecture, the processing units are separated from the memory units, the so-called von-Neumann bottleneck. The movement of data between processing unit and memory leads to significant costs in latency and energy. For solving the bottleneck of von-Neumann architecture, in-memory computing (IMC) paradigms are proposed [2]. One of the promising candidates for IMC paradigms exploits memristive devices as functional memory and computing cells [3], [4]. Memristive devices store the information in resistance states, and can be switched among them by applying correpsonding voltage stimuli. Memristive devices show prospects as low power and high-density memory as well as in IMC paradigms [5].

For realizing memristive in-memory computing (mIMC), stateful and sequential logic operations have been proposed. Stateful logic can be implemented by utilizing the resistance of the memristive devices as logic input and output. The most popular representatives of stateful memristive logic families are material implication (IMPLY) [6] [7] and memristor-aided logic (MAGIC) [8] [9]. Recently, MAGIC was demonstrated experimentally using memristive devices based on the valence change mechanism (VCM) [9]. In the investigated VCM cells the SET voltage, which switches the device from a high resistive state (HRS) to a low resistive state (LRS), is lower than the RESET voltage, which triggers the opposite resistance transition. Due to this property, the original MAGIC NOR gate failed. Thus, the authors of the study proposed two new MAGIC gates, i.e. the MAGIC NIMP and the MAGIC OR gate, and demonstrated their functionality experimentally [9]. In this work, the realization of MAGIC utilizing analog memristors is investigated using circuit simulations in the Cadence-Virtuoso framework. Here, a $BiFeO_3$ (BFO)-based memristive device [10] [11] is adopted as an example of an analog memristor in the MAGIC gate. The BFO memristive devices have been successfully applied in the application of in-memory computing [12], and in the emulation of artificial synapses in neuronal networks [13]. In this work, it is firstly shown in Section II that the previously proposed MAGIC gate does not work correctly with analog-switching BFO devices. Based on the failure analysis of these gates and the unique switching characteristics of the BFO devices, two functional MAGIC gates based on analog BFO memristors are proposed in this work in Section III. The correct gate operations are validated using simulations.

II. MEMRISTOR-AIDED LOGIC

MAGIC is a memristive logic family that realizes stateful IMC. As shown in the typical MAGIC circuitry in Fig. 1a, a 2-input MAGIC gate is illustrated, where two input memristors A and B are combined in parallel, and then connected in

series with one output memristor C. It is important to note that the two input devices are connected in an antiserial manner with the output device. MAGIC was developed for bipolar switching devices that switch between the LRS and HRS using opposite voltage polarities, the input devices are biased in SET polarity while the output device is biased in RESET polarity or vice versa depending on the implemented gate. Due to the circuit topology of the MAGIC gate, it is convenient to realize n-input MAGIC gates in a memristive crossbar on one line.

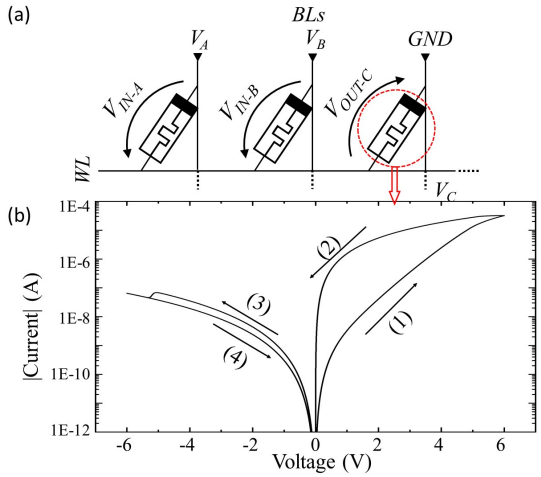

Fig. 1. (a) Schematic of a two-input MAGIC gate within a crossbar. The Au top electrodes (TEs) of memristors are connected in WL, and the Pt bottom electrodes (BEs) are connected in BLs. (b) $I-V$ characteristics of the simulated BFO memristor. The LRS (HRS) of the cell can be SET (RESET) by sourcing a positive (negative) pulse to the Au of the Au/BFO/Pt memristor. The bias applied for recording the IV characteristics are sourced to WL through individual device.

A. Modeling of MAGIC gates based on analog memristors

For analyzing the MAGIC logic gates as shown in Fig. 1a, a simulator in Cadence Virtuoso is developed by utilizing the memristive model based on the analog Au/BFO/Pt memristive device [14]. The mathematical model developed for analog Au/BFO/Pt memristive device with corresponding parameters from reference [14] is applied in this work. The Au TEs of simulated BFO devices are connected in the same WL, whereas the Pt BEs are connected in BLs. Hence, the biases V_{A} and V_{B} are applied to the Pt electrode of the input devices A and B, respectively. The voltage drop V_{C} over the output memristor C has the reversed sign of V_{A} and V_{B}. A voltage pulse with an amplitude of +6 V/-6 V applied to the Pt electrode, while the Au electrode is set to GND, switches the output device to the HRS/LRS. Thus, in the MAGIC gate topology +6 V/-6 V is applied as V_{A} and V_{B} at the bit line (BL) terminals of the input memristors A and B simultaneously, whereas the BL terminal connecting the output device is grounded, in order to SET/RESET the output device. The HRS of the analog BFO memristor is defined as logic '0' and the LRS as logic '1'. During MAGIC circuit simulation, the device-to-device (D2D) and cycle-to-cycle (C2C) variations of the memristive devices are not considered.

B. MAGIC NIMP gate by using analog memristors

For implementing the MAGIC gates, the input memristors A and B are initialized to the corresponding states according to the truth tables of Boolean logic gates, i.e. case (0, 0), Case (0, 1), Case (1, 0), and Case (1, 1) as shown on the left side in Fig. 2. For the MAGIC NIMP gate implementation, the output memristor C is initialized to HRS. After initializing the input memristors A, B, and output memristor C into the corresponding states, the MAGIC pulses V_{A} = 6 V and V_{B} = 2 V are applied for implementing the individual cases from MAGIC NIMP gate, respectively.

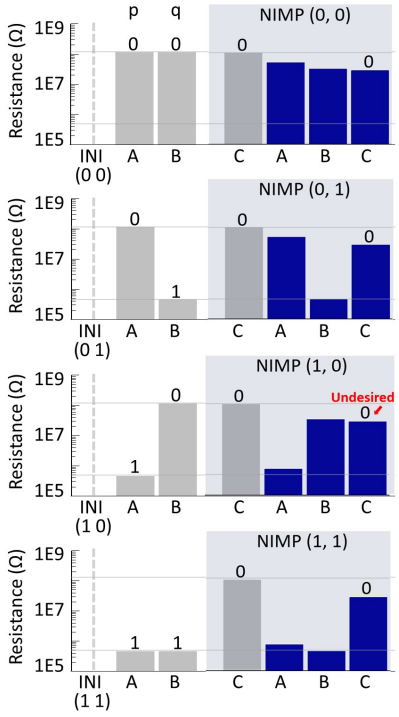

Fig. 2. Simulation of MAGIC NIMP gate based on circuit topology in Fig. 1 by using BFO based memristive models. The horizontal grey lines in each logical case (0, 0), case (0, 1), case (1, 0), and case (1, 1) indicate the initialized HRS and LRS values in input memristors A and B.

The simulation resistance results of input and output memristors of NIMP gate are demonstrated in Fig. 2 in blue shadowed region. The x-axis represents the cell name (memristor A, B or C) or an operation (initialization or gate evaluation) and the y-axis represents the measured resistance in logarithmic scale.

As can be seen in the simulated resistance results in blue bars in Fig. 2, the resistance values of the output memristor C are slightly decreased after applying the MAGIC pluses V_{A} = 6 V and V_{B} = 2 V in the NIMP gate in comparison to the initial HRS values, but still remain at a high resistive state for all 4 NIMP cases (i.e. logic '0'). Thus, it leads to the incorrect logic output in NIMP (1, 0) according to the desired truth table of NIMP gate and results in logical failure. Additionally, it is demonstrated that the resistance states of input memristors A and B are changed after applying the MAGIC pulses in

comparison to their initial resistance states, which indicates a significant input drift issue of the initialization states of analog input memristors.

III. NEW MAGIC GATES

In this section, the instability of the resistance states in the input memristors A and B, observed while implementing MAGIC NIMP gate, is studied. By solving this input drift issue, a novel MAGIC NOR gate and a novel -P gate are successfully demonstrated.

A. Study of the input drift of analog memristors

The observed input drift issue during operating MAGIC gates by using analog BFO memristors in Fig.2 is majorly caused by the following two reasons: (1) Analog memristors, in general, can be gradually switched between two resistance states, i.e. HRS and LRS, and do not show an abrupt transition between them. (Thus, multi-level resistance states can be easily adjusted in the analog memristive devices.) A resistance margin is usually determined for analog memristor to distinguish HRS and LRS, and a reading bias is then determined which shall not change the resistance state while applied acoss the analog memristor. In comparison to that, the digital memristors are switched to LRS or HRS only if the biases over the cells exceed the SET or RESET threshold biases, which depend on the timescale of the experiment. By sourcing the high MAGIC pulses to analog memristor (normally much higher than the reading bias), for all operations, the resistance drift of the analog input memristors is unavoidable. (2) The input drift issue while operating MAGIC NIMP gate is caused by the current blocking effect at negative voltages. As shown in Fig. 1b, the device exhibits always a high resistance in the negative bias region. While applying positive MAGIC pulses V_{A} and V_{B} to the Pt electrode (here the BL terminal) of the input memristors A and B. Due to such current blocking effect, the negative MAGIC pulses V_{A} and V_{B} shall be applied for performing MAGIC gate. Nevertheless, MAGIC NIMP gate still cannot be realized under negative MAGIC pulses as the output memristor C performs a RESET operation in this case.

Furthermore, the bias over the output memristor C $V_{\mathrm{OUT\text{-}C}}$ while implementing the NIMP logical operation is examined for the cases (1, 0) and (1, 1). As shown in Tab. I, the positive MAGIC pulses V_{A} and V_{B} in the range between 0 V and 7 V are chosen. The combinations between V_{A} and V_{B}, which are equal to 0 V, 2 V and 4 V are omitted due to the insufficient biases to change the resistance states of the BFO memristors. As illustrated in Tab. I, the highest $V_{\mathrm{OUT\text{-}C}}$ value in NIMP case (1, 0) under bias combinations V_{A} = V_{B} = 2.10 V cannot switch output memristor C into LRS, i.e. cannot fulfill the requirement of NIMP gate. The simulated $V_{\mathrm{OUT\text{-}C}}$ values are comparable in both NIMP cases accordingly. Such low $V_{\mathrm{OUT\text{-}C}}$ values prove again the blocking effect of bipolar switching dynamics of the BFO memristor.

In order to overcome the observed current blocking issue, instead of positive MAGIC pulses, we apply the negative

TABLE I
SIMULATION RESULTS OF BIAS OVER OUTPUT MEMRISTOR C $V_{\mathrm{OUT\text{-}C}}$ UNDER MAGIC PULSES V_{A} AND V_{B} = 0 V, 2 V, 4 V, 5 V, 6 V AND 7 V FOR MAGIC (A) NIMP (1, 0) AND (B) NIMP (1, 1).

(A) NIMP (1, 0)	V_{B} **(V)**					
	0	2	4	5	6	7
V_{A} = 0 V	-	-	-	0.14	0.18	0.23
V_{A} = 2 V	-	-	-	1.38	1.69	1.69
V_{A} = 4 V	-	-	-	1.51	1.75	1.73
V_{A} = 5 V	1.12	1.41	1.52	1.66	1.83	1.81
V_{A} = 6 V	1.42	1.79	1.83	1.84	1.96	1.94
V_{A} = 7 V	1.38	1.78	1.91	2.00	2.10	2.10
(B) NIMP (1, 1)	V_{B} **(V)**					
	0	2	4	5	6	7
V_{A} = 0 V	-	-	-	0.18	0.18	0.23
V_{A} = 2 V	-	-	-	1.41	1.83	1.89
V_{A} = 4 V	-	-	-	1.53	1.84	1.94
V_{A} = 5 V	0.18	1.41	1.53	1.67	1.85	2.00
V_{A} = 6 V	0.18	1.84	1.84	1.85	2.02	2.10
V_{A} = 7 V	0.23	1.89	1.94	2.00	2.10	2.19

TABLE II
SIMULATION RESULTS OF THE BIAS OVER THE OUTPUT MEMRISTOR C $V_{\mathrm{OUT\text{-}C}}$ UNDER MAGIC PULSES V_{A} AND V_{B} = 0 V, -2 V, -4 V, -5 V, -6 V AND -7 V FOR MAGIC (A) NIMP (1, 0) AND (B) NIMP (1, 1).

(A) NIMP (1, 0)	V_{B} **(V)**					
	0	-2	-4	-5	-6	-7
V_{A} = 0 V	-	-	-	-3.34	-4.03	-4.79
V_{A} = -2 V	-	-	-	-3.58	-4.24	-5.00
V_{A} = -4 V	-	-	-	-3.91	-4.29	-5.22
V_{A} = -5 V	-4.80	-4.84	-4.86	-4.86	-4.90	-5.31
V_{A} = -6 V	-5.74	-5.78	-5.81	-5.82	-5.82	-5.85
V_{A} = -7 V	-6.67	-6.72	-6.75	-6.76	-6.77	-6.77
(B) NIMP (1, 1)	V_{B} **(V)**					
	0	-2	-4	-5	-6	-7
V_{A} = 0 V	-	-	-	-4.76	-5.74	-6.57
V_{A} = -2 V	-	-	-	-4.84	-5.77	-6.61
V_{A} = -4 V	-	-	-	-4.86	-5.81	-6.66
V_{A} = -5 V	-4.76	-4.84	-4.86	-4.91	-5.82	-6.76
V_{A} = -6 V	-5.74	-5.77	-5.81	-5.82	-5.87	-6.67
V_{A} = -7 V	-6.57	-6.61	-6.66	-6.76	-6.67	-6.74

MAGIC pulses as demonstrated in Tab. II. By utilizing negative MAGIC pulses (corresponding to positive biases applied to the Au electrodes), both input memristors A and B are operated in the positive bias region. As shown in Tab. II, it is possible to distinguish the simulated $V_{\mathrm{OUT\text{-}C}}$ values between NIMP case (1, 0) and NIMP case (1, 1), e.g. under V_{A} = -6 V, and V_{B} = -2 V. Therefore, distinguishable $V_{\mathrm{OUT\text{-}C}}$ values indicate that the initialized LRS or HRS of the input memristors A and B are recognized and a possible resistance margin can be found.

B. MAGIC NOR and MAGIC -P

As discussed earlier, applying negative MAGIC pulses V_{A} and V_{B} can effectively solve the blocking effect of the input pulses while operating the MAGIC circuit topology and performing logical combinations by utilizing analog bipolar-switching BFO memristors.

For implementing the MAGIC NOR and MAGIC -P gates, the input memristors A and B are initialized to the correspond-

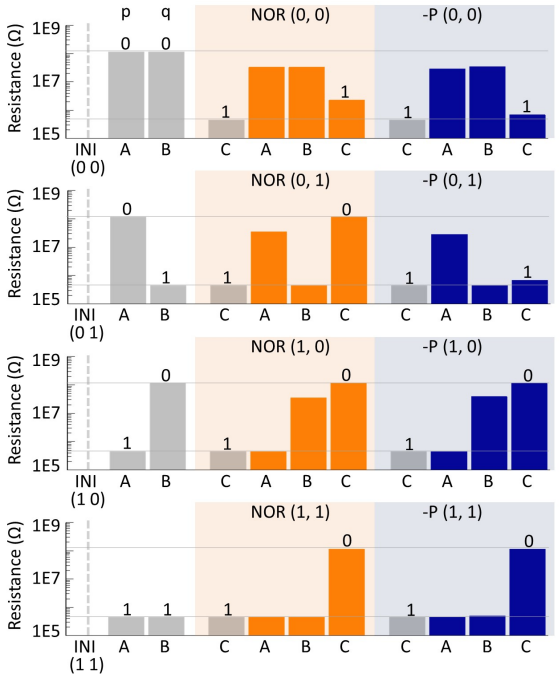

Fig. 3. Simulation of MAGIC NOR and -P gates based on circuit topology in Fig. 1 by using BFO based memristive models. The horizontal grey lines in each logical case (0, 0), case (0, 1), case (1, 0), and case (1, 1) indicate the initialized HRS and LRS values in input memristors A and B.

ing resistance states according to all 4 logic combinations as shown on the left side in Fig. 3. The output memristor C is initialized to the LRS. According to the test protocol, the MAGIC pulses V_A = V_B = -5 V and V_A = -6 V / $_B$ = -2V are applied for implementing the individual cases from MAGIC NOR gate and MAGIC -P gate, respectively.

The simulation resistance results of input and output memristors of MAGIC NOR and -P gates are demonstrated in Fig. 3 in orange and blue bars, respectively. As can be seen in the simulated resistance results in the orange and blue shadowed region in Fig. 3, the resistance values of the output memristor C before and after the MAGIC operations for the implementation of NOR and -P gates are demonstrated, respectively. Despite slight resistance variations, the resistance results of the output memristor C for MAGIC NOR and -P gates show the correct logic operation. Note that such resistance variations of the output memristor C in the logical state '0' or the logical state '1' are common for emerging resistance based memory devices [9]. Here, a clear margin (at least one order of magnitude) in the resistance between logical states '0' and '1' can be found, which indicates a reliable MAGIC logic implementation by applying negative MAGIC pulses. Furthermore, besides the resistance variability of the output memristor C, the input drift issue on the input memristors A and B is not alleviated but significantly mitigated in comparison to the implementation under positive MAGIC input pulses in all 4 logic cases.

IV. CONCLUSIONS

In this work, the limitations of executing MAGIC logic gate by using analog memristors, i.e. input drift and blocking effect, are demonstrated and studied while implementing MAGIC NIMP gate in the Cadence-Virtuoso by exploiting analog BFO memristors. Despite the unavoidable input instability in analog memristors during MAGIC operation, in order to overcome the current blocking issue, the MAGIC NOR and -P gates are successfully demonstrated under negative MAGIC pulses. This work enables stateful logic based on MAGIC in analog memristors and leads the way for further study on novel logic family development based on analog memristors.

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