Methodologies of Loop Offset voltage Trimming for Inverting-Buck-Boost for AMOLED Display Application

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Abstract— Methodologies of loop offset voltage trimming are presented in this paper for an inverting-Buck-Boost (IBB) having a wide output voltage (V_{NEG}) range (-0.9V to -5.3V) used in an AMOLED display driver. Furthermore, the circuit is proposed and analyzed to meet the brightness control requirement of the AMOLED display. The error contribution from each sub-blocks of the brightness control circuit to V_{NEG} is noted, and efficient ways of trimming the output voltage are analyzed. Achieving 0.3% of trimmed accuracy becomes challenging with the optimum number of trim bits as the magnitude of V_{NEG} voltage reduces. Three different ways of trimming the V_{NEG}, namely; three-step trimming, two-point trimming, and three-point trimming, are proposed and compared in terms of complexity and accuracy. The proposed methodologies of trimming are implemented for Inverting-Buck-Boost in BCD-180nm technology. Three-step trimming uses 17 bits (5-6-6 bits) resistor trimming and has the worst accuracy of ±0.17% across V_{NEG}. Two-point trimming uses 11 bits (6-5 bits) and has the worst accuracy of ±0.3%, whereas the three-point trimming uses only 14bits (6-4-4 bits) and has the worst accuracy of ±0.21%.

Keywords—Inverting Buck-Boost, offset trimming, DC-DC converter loop offset trimming, AMOLED display driver.

I. INTRODUCTION

AMOLED is a display technology and stands for Active Matrix Organic Light-Emitting Diodes. AMOLED screens are widely used in mobiles, laptops, and smartwatches. AMOLED display requires two positive and one negative supply rails. Boost converters drive two positive supply rails (V_{POS} & AV_{DD}), and Inverting-Buck-Boost drives the negative supply rail (V_{NEG}) in battery-operated products. Positive supply rails are fixed, and the negative supply rail is digitally programmable. The brightness of AMOLED display is controlled by changing the negative supply rail.

It is observed that in most of the DC-DC converters, the offset of gm-amplifier adds inaccuracy to the output voltage. This inaccuracy can be trimmed simply by changing the feedback resistor network, but in IBB, there are multiple blocks used to meet the brightness control requirement of AMOLED display. Offset voltages of these various blocks would be scaled and added to the output loop offset voltage, which will add significant inaccuracy at the output voltage. It makes the trimming of loop offset voltage relatively complicated. Also, the trim range is much higher and needs a more significant number of trim bits to meet the required accuracy, and most importantly, trimming cannot be done in a single step. It involves multiple steps and tapping of many nodes for measurement. This complication makes loop offset voltage trimming in IBB is worth optimizing. During the literature survey, it is observed that there are no papers reported till now that address the complication involved in loop offset voltage trimming for DC-DC converters when multiple blocks have a contribution to the loop offset voltage. This is the first paper that analyzes the loop offset voltage of IBB and provides three solutions for the trimming.

In this paper, the circuit is proposed to meet various requirements of V_{NEG} rail, and three different ways of trimming loop offset voltage of IBB are presented. Section II, III and IV elaborate on details of Three-Step Trimming, Two-Point trimming, and Three-Point trimming, respectively. The results of these three methods of trimming are presented in section V, followed by the conclusion in Section VI.

Figure-1 is the block diagram of the current-mode control loop of IBB. The highlighted circuit in the box is the proposed circuit to carry out following functionalities, i) To level shift V_{NEG} to a positive voltage to compared it with positive reference voltage for regulation, ii) To implement digital programmability of V_{NEG}, iii) To have RC charging/discharging behavior of V_{NEG} during the transition from one voltage to another voltage. R_6 and R_7 resistors, together with XBUFF amplifier, do level shifting of VNEG to a positive voltage. In a steady-state of operation, negative feedback will ensure V_{FB} regulated to V_{REF2}. The gain of the XBUFF amplifier is a design parameter. C_{ext}, together with the R_3 resistor implement RC settling behavior of V_{NEG}. C_{ext} would be placed outside the IC. Time constant of V_{NEG} settling is R_3*C_{ext}, assuming output resistance of DAC is much smaller than R_3 i.e. R_{out_DAC} << R_3. Digital programmability of V_{NEG} is implemented using resistor DAC. Reference voltage input (V_{REF2}) to Gm amplifier is derived from DAC. V_{GM_OFS}, V_{XBUF_OFS} and $V_{DAC\_AMP\_OFS}$ are offset voltage of Gm amplifier, buffer amplifier and DAC amplifier, respectively. These offset voltages are due to the mismatch of various internal devices and due to process variations. $V_{NEG\_DAC\_OFS}$, $V_{NEG\_XBUF\_OFS}$ and $V_{NEG\_GMAMP\_OFS}$ are voltage at V_{NEG} due to V_{GM_OFS}, V_{XBUF_OFS} and $V_{DAC\_AMP\_OFS}$ respectively.

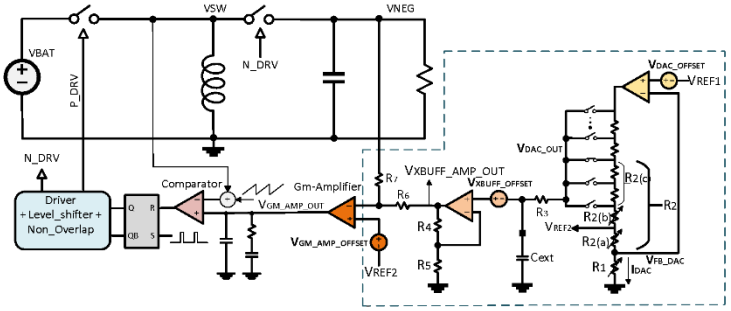

Figure 1: IBB current mode loop with level shifter and its offset voltages

Offset voltage contribution of different sources at output voltage (V_{NEG}) is,

$$V_{NEG} = -\frac{R_7}{R_6} * \left(1+\frac{R_4}{R_5}\right) * \left(1+\frac{R_2}{R_1}\right) * \left(V_{REF1} + V_{DAC_{OFFSET}}\right) - \frac{R_7}{R_6} * \left(1+\frac{R_4}{R_5}\right) * V_{XBUF_{OFFSET}} + \left(1+\frac{R_7}{R_6}\right) * \left(V_{REF2} + V_{GM\_AMP_{OFFSET}}\right) \text{-- (1)}$$

II. Three –Step Loop offset Trimming:

In this method, three different resistors are trimmed in three steps. The gain of the XBUFF amplifier is chosen one in this method to reduce the trimming steps; otherwise, it needs two more extra steps to cancel out offset of XBUFF amplifier for trimming R_4 and R_5 separately. The circuit setup for each trimming step is shown in Figure-2. In step-1, R1 resistor is trimmed to R'_1 by looking at voltage difference between DAC output and V_{FB} nodes to correct the change in current in resistor ladder to $\frac{V_{REF1}}{R1}$ by making $(V_{DAC\_OUT} - V_{REF1}) = \frac{R2}{R1} * V_{REF1}$. This will eventually bring the input-referred offset of DAC amplifier from the input terminal to the output terminal of DAC. After step-1, the output voltage of DAC is

$$V_{DAC\_OUT} = \left(1+\frac{R_2}{R'_1}\right) * \left(V_{REF1} + V_{DAC\_OFS}\right) \text{ ----(2)}$$

In Step-2, the gm-amplifier is configured in a unit feedback configuration, as shown in figure-2 (b). $R_{2\,(a)}$ is trimmed to R'_2, and the output of the Gm-amplifier is measured and brought back to V_{REF2} to trim offset of gm amplifier. In this step, the offset of the gm amplifier is separately trimmed, and due to this, offset of gm amplifier could add or subtract to the DAC output voltage depending on the polarity of the offset voltage. After step-2, DAC output has offset of DAC amplifier and offset of Gm amplifier. DAC output voltage after step-2 is,

$$V_{DAC\_OUT} = \left(1+\frac{R'_2}{R'_1}\right) * \left(V_{REF1} + V_{DAC\_OFS}\right) \text{ ----(3)}$$

In Step-3, $R_{2(b)}$ resistor is varied to trim XBUFF amplifier offset, DAC offset, and residue of GM amplifier offset present at the output node of DAC. Figure-2 (c) shows the trim setup. The Gm amplifier is configured in the open-loop configuration. It acts as a comparator and does comparison V_{NEG} and V_{REF2}. V_{NEG} node is varied from $V_{NEG} + \Delta V_{NEG}$ to $V_{NEG} - \Delta V_{NEG}$ (where ΔV_{NEG} is the total variation (3σ) of V_{NEG}). Trimming of $R2_{(b)}$ resistor is done to bring V_{NEG} back to default voltage and repeat the process to verify the same. V_{NEG} after trimming $R_{2(b)}$ is,

$$V_{NEG} = \left(V_{REF2} - V_{XBUF\_OUT}\right) * \frac{R_7}{R_6} + V_{REF2} \text{----(4)}$$

$$V_{XBUF_{OUT}} = \left(1+\frac{R''_2}{R'_1}\right) * \left(V_{REF} + V_{DAC_{OST}}\right) + V_{GM_{OFS}} + V_{XBUF_{OFS}}$$

$$R''_2 = R'_2 \pm \frac{\left(V_{Gm\_AMP\_OFFSET} + V_{IP33\_AMP\_OFFSET} + V_{DAC\_OFFSET}\right)}{I_{DAC}}$$

In three-step trimming method, V_{REF2}, XBUFF gain and DAC gain should be chosen as per below equation to ensure all trimming range is covered,

$$V_{REF1} < (V_{REF2} - V_{TRIM1}), (V_{REF2} + V_{TRIM1}) < (V_{DACmin} - V_{TRIM2})$$

Where V_{TRIM2} is 3σ value of offset voltage of Gm-amplifier and DAC amplifier, V_{TRIM3} is 3σ value of offset voltage of Gm-amplifier, DAC amplifier, and XBUFF amplifier.

III. Two – Point Loop offset Trimming:

In this method, trimming is done at two different values of V_{NEG} to ensure the required accuracy is achieved for the entire range of V_{NEG}. After trimming, trim bits are stored internally and changed accordingly with V_{NEG} programming bits. Figure-3 shows the test setup of Two-Point loop offset trimming. In this method, V_{REF2} is derived from resistor DAC same as in Three-Step trimming. The Gm amplifier is configured in an open-loop configuration. It acts as a comparator and makes the comparison of scaled V_{NEG} and V_{REF2}.

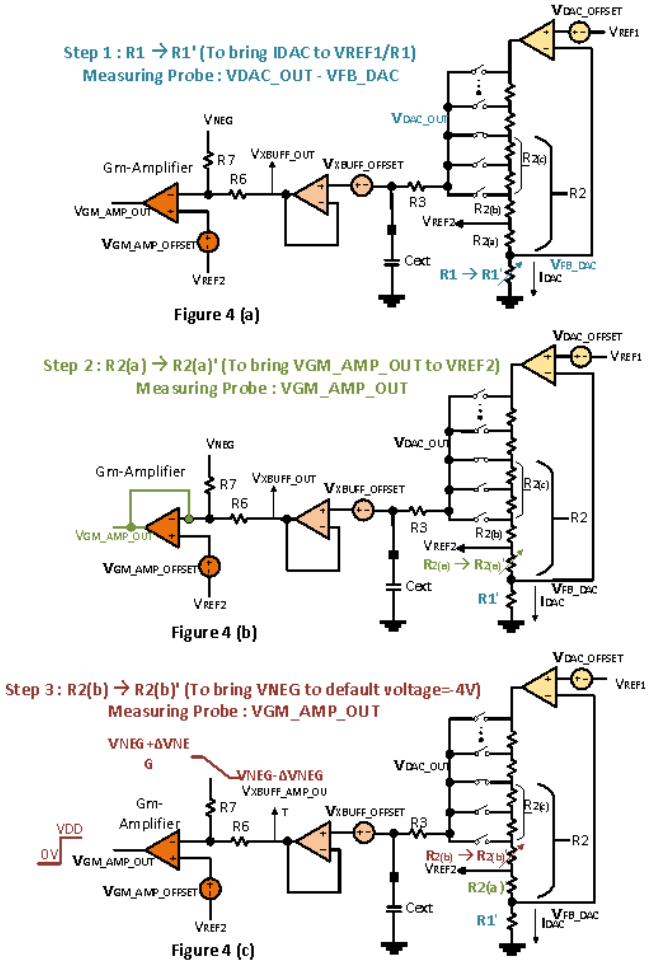

Figure 2: Test setup of Three-point loop offset trimming

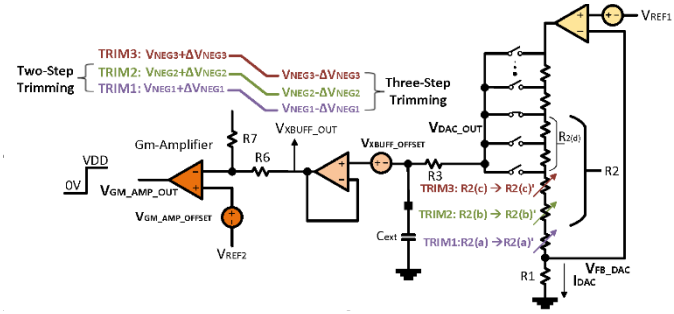

Figure 3: Test setup of Two-point and Three-point Loop offset trimming is shown in a single figure

In step-1, DAC is programmed to get default V_{NEG1}. V_{NEG} node is varied from $V_{NEG1} + \Delta V_{NEG1}$ to $V_{NEG1} - \Delta V_{NEG1}$. Where ΔV_{NEG1} is a total variation (3σ) of V_{NEG}. If there is no offset, then the Gm amplifier output will switch from low to high at default V_{NEG1} voltage, or else Gm amplifier output will change as per equation-1. $R_{2(a)}$ resistor is trimmed to cancel out the offset at V_{NEG} at default voltage. These bits are stored internally and used for the entire range of V_{NEG}. During second step trimming, step-1 trim bits are kept as it is, and DAC is configured at appropriate V_{NEG} (say V_{NEG2}=-1V) to get the least variation across V_{NEG} after trimming resistor $R_{2(b)}$. The trim procedure is the same for trimming $R_{2(b)}$ but at V_{NEG2} value. Trim-2 bits are stored internally and used for selected voltages of V_{NEG} for improving accuracy.

IV. Three-Point Loop offset Trimming:

In this method, trimming is done at three different values of V_{NEG} to ensure that the required accuracy is achieved for the entire range of V_{NEG}. After trimming, trim bits are stored internally and changed appropriately with V_{NEG} programming bits. Figure-3 shows the test setup for this method.

V. Results and Discussion

Test setup shown in Figure 2 and 3 are used for capturing the below results. All test cases are simulated by forcing appropriate external offset voltages and are verified with equations 1, 2, 3, and 4. The range of output voltage of IBB is from -0.9V to -5.3V, and it is programmable by the digital interface at a step of 100mV with 45 digital levels (6 bits). The input voltage range is 2.5V to 4.8V. The implemented IBB can supply the maximum load current of 400mA with an efficiency of more than 89%.

The input reference voltage (V_{REF1}) of resistor DAC is chosen 0.8V, and Gm-amplifier is chosen V_{REF2}=0.9V. The output voltage of DAC for the given range of V_{NEG} (-0.9V/-5.3V) is chosen 1.08V to 1.52V at the step of 10mV with 45 digital levels. This is done to ensure that there is sufficient range of voltage is available to trim offset voltage of DAC, GM amplifier and IBB loop as per equation-1, $V_{REF1} < (V_{REF2} - V_{TRIM1})$ & $(V_{REF2} + V_{TRIM1}) < (V_{DACmin} - V_{TRIM2})$. DAC resistor current is chosen 1.6uA. The gain of XBUF is chosen one.

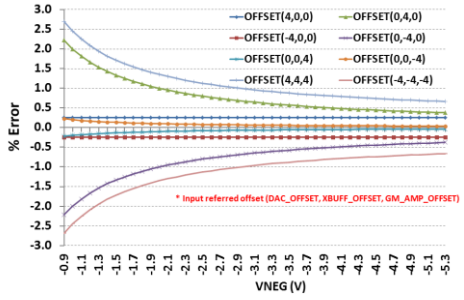

Figure-4: Percentage error at V_{NEG} due to offset voltages of sub-blocks

R_6=240kΩ and R_7=2.4MΩ are selected to fit the output voltage range of DAC to a scale, which is more than 1V ($V_{DACmin} > V_{REF2} + V_{TRIM}$) and lower than the minimum supply voltage. ±3σ value of offset voltage of resistor DAC amplifier, Gm amplifier, and XBUF amplifier is ±4mV. Figure-4 shows the percentage error in V_{NEG} because of different offset voltages.

a) Results of Three-Step loop offset trimming

V_{NEG} is programmed to default voltage of -4V. Difference between V_{DAC_OUT} and V_{FB_DAC} (V_{DIFF} = V_{DAC_OUT} - V_{FB_DAC}) is observed, and it is brought back to 0.59V by changing R1 resistor. In Step-2, the trimming of $R_{2(b)}$ resistor is done to bring the output of unit feedback - gm amplifier to 0.9V. In Step-3, $R_{2(b)}$ is trimmed to bring VNEG back to the default voltage. Table-1 (a), (b), (c) shows the trim resistor and its trim bits after each step.

RES $R_{2(a)}$ (in kΩ)	DIG BITS	DAC Offset (in mV)	XBUF Offset (in mV)	GM Amp Offset (in mV)	V_{DIFF} Before trim (in V)	V_{DIFF} After trim (in V)
2.5	16	4	0	0	0.593	0.590
-2.5	-16	-4	0	0	0.587	0.590
0	0	0	4	0	0.590	0.590
0	0	0	-4	0	0.590	0.590
0	0	0	0	4	0.590	0.590
0	0	0	0	-4	0.590	0.590
2.5	16	4	4	-4	0.593	0.590
-2.5	-16	-4	-4	4	0.587	0.590

Table-1 (a): Trim table after Step-1of Three-Step trimming

RES $R_{2(b)}$ (in KΩ)	DIG BITS	DAC Offset (in mV)	XBUF Offset (in mV)	GM Amp Offset (in mV)	GM_OUT Before trim (in V)	GM_OUT After trim (in V)
-2.5	-8	4	0	0	904	900
2.5	8	-4	0	0	896	900
0	0	0	4	0	900	900
0	0	0	-4	0	900	900
-2.5	-8	0	0	4	904	900
2.5	8	0	0	-4	896	900
-5	-16	4	4	4	908	900
5	16	-4	-4	-4	892	900

Table-1(b): Step-2 of Three-Step trimming

RES $R_{2(b)}$ (in KΩ)	DIG BITS	DAC Offset (in mV)	XBUF Offset (in mV)	GM Amp Offset (in mV)	V_{NEG} Before trim (in V)	V_{NEG} After trim (in V)
0	0	4	0	0	-4.000	-4.000
0	0	-4	0	0	-4.000	-4.000
-2.5	-16	0	4	0	-4.040	-4.000
2.5	16	0	-4	0	-3.960	-4.000
2.5	16	0	0	4	-3.960	-4.000
-2.5	-16	0	0	-4	-4.040	-4.000
-5	-32	4	4	-4	-4.080	-4.000
5	32	-4	-4	4	-3.920	-4.000

Table-1(c): Step-3 of Three-Step trimming

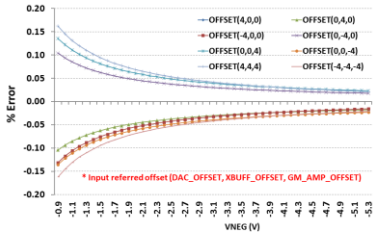

Figure-5: Error at V_{NEG} after Three-Step trimming due to half LSB

Figure-5 shows the error at V_{NEG} after three-step trimming due to half LSB. The maximum error of 0.17% is seen at V_{NEG} = -0.9V due to half LSB voltage at each trimming step.

b) Results of Two-Point loop offset trimming

In two-point trimming, trimming is done at V_{NEG} = -3.5V and V_{NEG} = -1V to reduce the percentage error across the V_{NEG} range. Error in V_{NEG} after step-1 and step-2 is shown in Figure-6(a) and Figure-6(b), respectively.

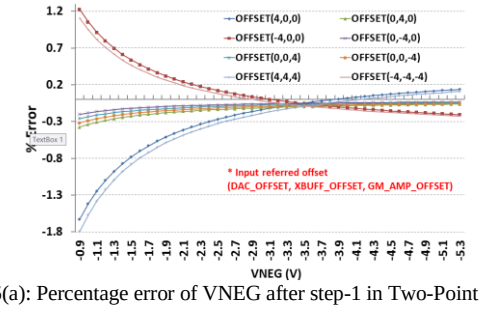

Figure-6(a): Percentage error of VNEG after step-1 in Two-Point trimming

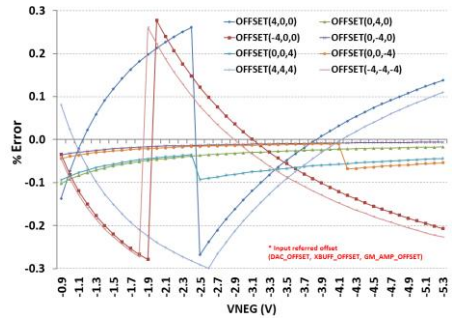

Figure-6(b): Percentage error of V_{NEG} after step-2 in Two-Point trimming

Two-Point trimming uses the same trim setup for both steps. $R_{2(a)}$ is trimmed with six bits in step-1and $R_{2(b)}$ is trimmed with five bits in step-2. Step-1 trim bits are used across V_{NEG}, whereas step-2 trim bits are used for -0.9V < V_{NEG} < -2V.

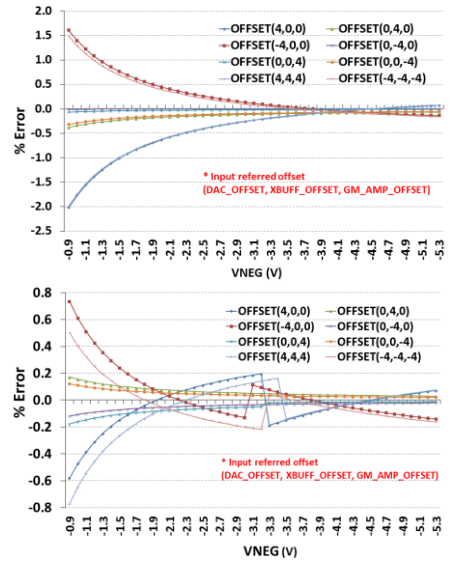

Figure-7 (a) & (b): Percentage error in VNEG after step-1 and step-2 in Three-Point trimming respectively

c) Results of Three-Point loop offset trimming

In three-point trimming, trimming is done at V_{NEG} = -4V, V_{NEG}=-2V and V_{NEG}=-1V. Error in V_{NEG} after step-1, step-2 and step-3 is shown in Figure-7(a), Figure-7(b) & Figure-7(c) respectively. $R_{2(a)}$, $R_{2(b)}$ and $R_{2(c)}$ are trimmed with six, four and four bits respectively. Step-1 trim bits are used across V_{NEG}, step-2 trim bits are used for -0.9V < V_{NEG} < -3.2V and step-3 trim bits are used for -0.9V < V_{NEG} < -1.5V. Comparison of trim mythologies is tabulated in Table-2.

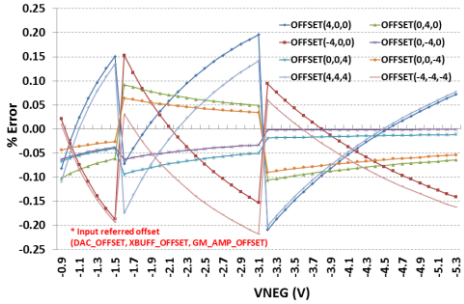

Figure-7 (c): Percentage error in V_{NEG} after step-3 in Three-Point trimming

Parameters	Three-Step trimming	Two-Point trimming	Three-Point trimming
Accuracy (%)	0.17	0.3	0.21
Trim bits	17	11	14
No of nodes brought outside for measurement	3 (DAC_VFB, DAC_OUT and GM_OUT)	1 (GM_OUT)	1 (GM_OUT)
Different trim-setup	3	1	1
IBB architecture having external programmable VNEG	Applicable	Not Applicable	Not Applicable

Table-2: Comparison of trim methodologies

VI. CONCLUSION

In this paper, the circuit is proposed to meet the AMOLED driver requirement for V_{NEG}. Three different ways of offset trimming, namely three-step, two-point, and three-point trimming is presented with clear-cut trimming steps and evident analytics. Three-step trimming is a conventional way of trimming the loop offset voltage, and error in this method is only because of half LSB voltages of each trim step. The test setup used in three-Step trimming is complex as compared to the other two techniques. Two-step and three-step trimming methodologies are unconventional ways of trimming the loop offset voltage. Three-point trimming uses a lesser number of bits and easier trim-setup as compared to the three-step trimming and achieves reasonable accuracy with a lesser number of bits.

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