A novel Approach for Extending the Bandwidth Limitation of Tracking-ADCs

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***Abstract*—A method for extending the bandwidth limitation of tracking ADCs is presented. It takes advantage of the conventional tracking approach regarding conversion speed. The proposed concept of generating reference steps improves the traditional tracking limits of the input signal slope. MATLAB evaluations of an ideal tracking ADC demonstrate the ability of the novel approach to extend the bandwidth. An implementation in a 65 nm process demonstrates the applicability. Verification by post layout simulation results offer an effective resolution of 6.47 bit at a sampling rate of 323 MS/s while consuming a power of 2.8 mW. Nonlinearity caused by internal mismatch or PVT variations can be compensated with an correction system. Compared to state-of-the-art SAR ADCs the proposed ADC matches the characteristics and advances the limitations of the conventional tracking ADC. A 94% digital implementation by standard cells and the ability to digital compensate nonlinearity demonstrate the excellent scalability with technology.**

I. Introduction

In recent years, the continuous scaling of integrated technologies has enabled the improvement of switching frequencies and energy efficiency for digital circuits, but analog circuits still require a large scale integration to enable a desired performance in terms of precision, gain or speed. As a consequence due to up scaling, analog components are not able to represent the full potential of the advantages in terms of area and power efficiency provided by these technologies. Especially the conversion of real world analog signals into corresponding, processable digital representations by an analog-to-digital-converter (ADC) demand for higher performing systems. In order to provide leading edge conversion speed and moderate resolution while handling short-channel effects, ADCs are implemented in a more and more digital way. Almost completely digital implementations as introduced in [1] or [2] directly benefit from the improved abilities and are able to apply techniques like time interleaving. Other approaches offer techniques, such as noise shaping due to oversampling for SAR ADCs [3] to boost the performance. Tracking type ADCs are a class of converters offering a signal conversion for every comparison with the analog input and thus achieve sampling rates at the switching speed limited of the used technology. However, a challenge is that the sampling scheme of a tracking ADC depends on the slope of the input signal and thus limits the input bandwidth [4]. Furthermore, performance reductions resulting in reduced ADC resolution arise due to short-channel implementations. To overcome these limitations this work introduces an novel tracking ADC in 65 nm technology which generates a faster reference signal for determining relative dependencies to the analog input signal based on the desired resolution. In addition the proposed concept offers the ability of a digital self-adaption by the measurement of the system nonlinearity caused by mismatch or PVT variations.

II. Basic Concept

A. Tracking ADC Sample Considerations

In the tracking ADC approach [5] the physical properties of the ADC-system based on resolution and total delay of the conversion loop (i.e. the minimum time needed for a sample) are decisive about the ability to convert the input signal. The basic tracking system in Fig. 1 is based on a continuous counting behavior and provides a reference voltage (V_{ref}) proportional to the actual counter value. A comparator decides if the actual reference voltage is higher or lower than the actual input voltage (V_{in}) and changes the counter polarity (i.e. up or down counting) based on this decision. In this way the system tracks the input signal and ideally converts with every change of the reference voltage. The maximum sample rate of the ADC is limited by the total internal system delay ($\tau_{\mathrm{d}} = \tau_1 + \tau_2 + \tau_3$) and is defined by the sum of the comparator delay (τ_1), the counter delay (τ_2) and the digital to analog converter (DAC) delay (τ_3). The resolution of the ADC is limited by the amount of the physical decision level of the comparator.

Due to the continuous tracking scheme the ADC system generates a comparison between the input signal (V_{in}) and the reference signal (V_{ref}) for every clock cycle of the counter (CLK). Ideally, every comparison provides a valid sample

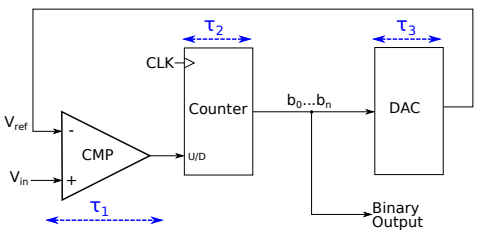


Fig. 1. Tracking ADC system overview and total system delay based on the sum of comparator delay (τ_1), counter delay (τ_2) and DAC delay (τ_3).

which would be the case for a static signal. In case of a dynamic signal it can happen, that the tracking ADC needs several clock cycle to validate a sample. The described behavior is based on the system properties regarding internal delay (τ_d) and minimum quantization level which is related to the slope of the input signal (V_in). Therefore, the slope of the input signal must respect the following condition described in [6]:

$$\left|\frac{d\,(V_\mathrm{in})}{dt}\right| \leq \frac{V_\mathrm{lsb}}{\tau_\mathrm{d}} \tag{1}$$

, where V_lsb is the minimum quantization level related to the comparator full-scale range and the resolution and τ_d is the internal system delay, that equals the counter clock $(f_\mathrm{clk})^{-1}$. In order to define the maximum bandwidth of the system the input signal is modeled by a sine wave with frequency f_in and peak-to-peak amplitude A_in.

Applying Eqn.(1) results in the relation between the input signal slope and the tracking ADC system specifications. In consideration if the maximum input signal slope, the maximum applicable frequency f_max (i.e the bandwidth) can be defined:

$$\begin{aligned} |A_\mathrm{in}\pi f_\mathrm{in}\cos(2\pi f_\mathrm{in}\cdot t)| &\leq \frac{V_\mathrm{lsb}}{\tau_\mathrm{d}} \\ \max\left(\cos(2\pi f_\mathrm{in}\cdot t)\right) &\leq \frac{V_\mathrm{lsb}}{A_\mathrm{in}\pi f_\mathrm{in}\tau_\mathrm{d}} \end{aligned} \tag{2}$$

Furthermore, the expression should be related to the overall system parameters regarding resolution (N) and counter clock frequency (f_clk) the estimation results in Eqn.(3). Therefore, A_in is related to the comparator full-scale range and the number of bit (N) and τ_d to the counter clock frequency f_clk.

$$f_\mathrm{max} = \frac{V_\mathrm{lsb}}{A_\mathrm{in}\pi\cdot\tau_\mathrm{d}} = \frac{f_\mathrm{clk}}{\pi\cdot(2^N-1)} \tag{3}$$

Eqn.(3) gives the input frequency limit to provide the desired resolution. If the Nyquist bandwidth needs to be considered, it is necessary to determine the maximum and minimum of the input sine wave. Hence, the time needed to reach the maximum voltage level. Based on the counter clock frequency and the resolution the time until reaching the maximum voltage level by continuous counting is decisive about the Nyquist frequency. Since the maximum and minimum of the input sine wave needs to be defined for a proper signal recovery, twice the maximum time needs to be considered. Eqn.(4) defines the Nyquist bandwidth (f_nyq) of the tracking ADC.

$$f_\mathrm{nyq} = \frac{f_\mathrm{clk}}{2\cdot(2^N-1)} \tag{4}$$

B. Extending the Tracking ADC Bandwidth Limitation

As derived in Eqn.(3) and Eqn.(4) the bandwidth limitations for a tracking ADC depend on the counter clock frequency (f_clk) which is related to the maximum system feedback delay (τ_d. The evaluation of both equations reveals the hypothesis to increase the counter frequency to extend

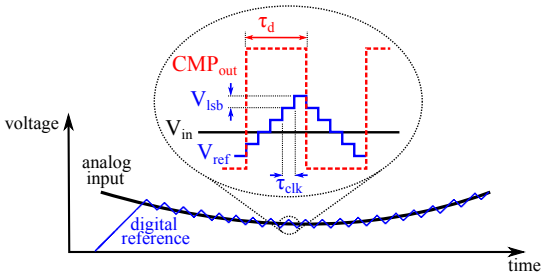
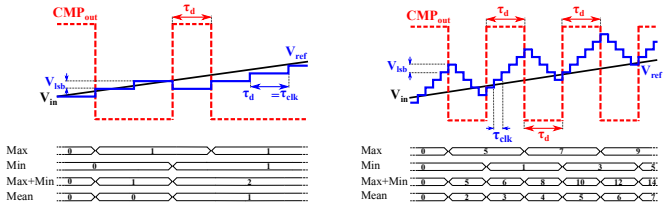


Fig. 2. Proposed sample scheme of the digital reference (V_ref) which oscillates around the analog input by generating a triangular shaped stair-step function.



(a) Traditional: $\tau_\mathrm{clk} = \tau_\mathrm{d}$. (b) Proposed: $\tau_\mathrm{clk} < \tau_\mathrm{d}$.

Fig. 3. Increased information density in (b) compared to the traditional tracking ADC (a).

the maximum bandwidth of the ADC. In the conventional tracking ADC approach the counter frequency is based on the system delay and thus defines the maximum sample rate of the ADC. If the counter frequency is increased, a higher slope of the reference voltage (V_ref) is generated as depicted in Eqn.(1). The basic principle is to generate a triangular stair-step function (V_ref) whose switching moments are specified by the slope of the input signal (V_in) and the internal system delay (τ_d). Fig. 2 illustrates an example of a resulting reference signal (V_ref) oscillating around the analog input signal by generating a triangular stair-step function.

In general, the proposed reference generation scheme allows a relative dependency between the analog input signal and the current reference count values based on the reference update rate (τ_clk) and the system delay (τ_d). Additionally, due to faster reference signal generation a higher slope generates more information compared to the conventional tracking ADC as depicted in Fig. 3. Based on the reference update rate, the triangular shape enables an improvement of the possible input signal slope. Both of the corresponding counter values found by comparator inversion (min, max of the alternating reference signal (V_ref)) can be used for providing a double data rate. Thus, there is no more need for bit-bobble as for the conventional tracking ADC approach [7].

In order to examine the derived equations Eqn.(3) and Eqn.(4) and the resulting hypothesis to increase the tracking ADC bandwidth by application of a faster counter frequency, an ideal tracking ADC system was developed in MATLAB. In this way the tracking ADC implemented in MATLAB is defined by the resolution (N), the system delay (τ_d) and the counter frequency (f_clk). The proof of concept is examined by the signal to noise ratio (SNR) of the ADC output signal once for the relation that $\tau_\mathrm{clk} = \tau_\mathrm{d}$ and once for the relation

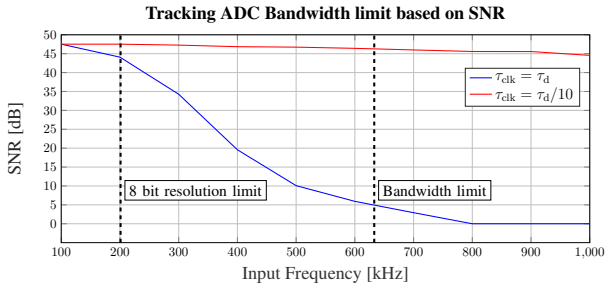


Fig. 4. SNR of conventional tracking ADC ($\tau_{\mathrm{clk}} = \tau_{\mathrm{d}}$) demonstrating the derived limitation compared to the proposed approach ($\tau_{\mathrm{clk}} = \tau_{\mathrm{d}}/10$).

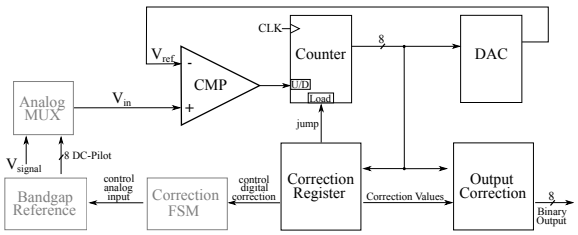


Fig. 5. Block diagram of the proposed tracking ADC with self-adaptive correction system.

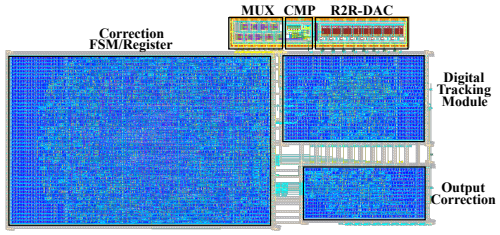


Fig. 6. Layout of the proposed ADC subdivided into functional blocks.

that $\tau_{\mathrm{clk}} = \tau_{\mathrm{d}}/10$. Fig. 4 demonstrates the improved SNR by applying a ten times faster counter clock τ_{clk} and shows the bandwidth limits of the conventional approach within the examined frequency range from 100 kHz - 1MHz. The 8 bit resolution limit is defined by Eqn.(3) considering twice the delay (τ_{d}) due to bit validation. The Nyqist bandwidth limit is defined by Eqn.(4).

III. System Architecture

A. Self Adaption Finite-State-Machine

Nonlinearity based on internal mismatch or external PVT variations affect the overall system delay and thus the relation between fixed reference signals and input signals. In order to determine the mismatch of the overall system delay, measurements in advance of the conversion are necessary for processing digital correction. The tracking ADC method allows to measure the analog system based on the DAC and comparator combination and relates the linearity deviations to a correction factor. Due to the triangular sampling scheme, the correction factors are related between time and absolute voltage and can be expressed in multiple of LSBs. It is expected that the ideal system offers a symmetric oscillation of the reference signal by applying an analog time-constant reference. Regarding the mismatch of the overall system delay, the nonlinearity causes the oscillation of the reference signal to be asymmetrical. Therefore, a Finite-State-Machine (FSM), acting as measurement system, has to calibrate the asymmetry before of the actual conversion. In this way, the measurement of 8 equally distributed constant analog pilot signals, generated by a bandgap reference, provides the information about the absolute deviation from the ideal digital representation. In subsequently steps, the deviations are linearized and stored in a correction register.

B. Proposed System Architecture

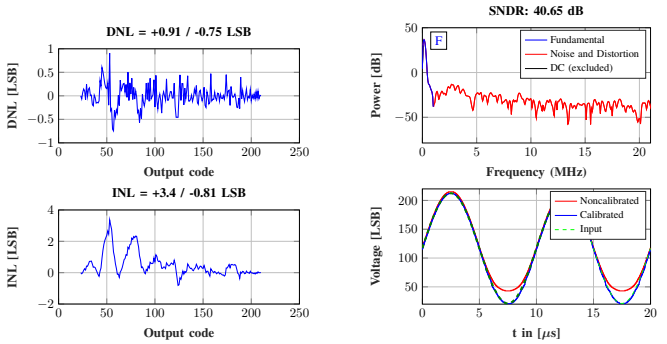
The architecture of the proposed tracking ADC is illustrated in Fig. 5. The counter represents the core system for reference generation. The combination of the DAC and the comparator represents the analog system components which has to be calibrated by digital operations. By expanding the topology with a correction FSM and an associated correction register the calibration operation is provided before the conversion. There are 8 equally distributed DC-pilot signals used for the ADC calibration generated by a bandgap reference. An analog multiplexer is controlled by the correction FSM and provides either the analog DC-pilot signals or the analog input signal to be converted.

IV. Implementation and Simulation Results

The proposed tracking ADC is implemented in a 65 nm technology and occupies a total area of 0.027 mm^2. The layout is shown in Fig. 6. The digital blocks are implemented by standard cell designs with automated synthesis and place-and-route tools providing PVT and Monte-Carlo stable layout designs. In order to exploit the digital performance of continuous scaled technologies, the ADC layout is based on a 94% digital implementation, since the remaining analog blocks (comparator/R2R-DAC combination) occupy an area of 0.0015 mm^2. In consideration of the required functional blocks for the basic concept without calibration, the total effective area of the combination of the analog part and the digital tracking module reduces to 0.0056 mm^2. The implementation of the bandgap reference layout is not to be considered as part of the ADC, since it should demonstrate the proof of concept by providing reference levels for calibration.

Calibration in advance and conversion are two separated operation modi which allows to enable or disable functional blocks related to the current ADC state. During calibration, every block of the ADC is used simultaneously which leads to a total power consumption of 3.65 mW. While conversion, the correction FSM and the bandgap reference are disabled and the simulated power consumption reduces to 2.8 mW for a reference generation frequency of $f_{\mathrm{clk}} = 1.66$ GHz.

The ADC has an input range of $V_{\mathrm{pk-pk}} = 1000$ mV. The bandwidth depends on the ability of the generated triangular function to track the input signal slope. Thus, for a reference generation frequency of 1.66 GHz, the bandwidth results in $BW = \left[(V_{\mathrm{pk-pk}}/V_{\mathrm{lsb}}) \cdot 2\tau_{\mathrm{clk}}\right]^{-1} = 3.9$ MHz. Fig. 7b compares



(a) DNL and INL (b) FFT Spectrum and IO-signals

Fig. 7. Post layout simulation of the static performance (DNL, INL) shown in (a) and dynamic performance (SNDR) shown in (b-top). A comparison between the input signal and the calibrated and noncalibrated output is shown in (b-bottom).

the input signal at 100 kHz (input) with the post layout simulation results of the converted signal without correction (noncalibrated) and the binary corrected digital signal (calibrated). It is obvious that the corrected signal represents a closer analog input representation than the simple converted signal (noncalibrated) and thus demonstrates the need and the functionality of the correction system.

The evaluations regarding FFT, INL and DNL are also based on the 100 kHz analog input sine wave with an input range of $V_{\mathrm{pk-pk}} = 1000\,\mathrm{mV}$. Fig. 7a illustrates the worst-case scenario of 0.91 LSB for the DNL and 3.4 LSB for the INL.A reduction of the input range towards 300 mV-1100 mV would offer a worst-case DNL < 0.5 LSB and a worst-case INL < 1 LSB. The evaluated FFT spectrum shown in Fig. 7b illustrates a signal-to-noise-and-distortion ratio (SNDR) of 40.65 dB which corresponds to an effective number of bits (ENOB) of 6.47 bit. In comparison, the converted signal without correction would result in an ENOB of 3.53 bit.

The sampling rate of the ADC was simulated to an average of 323 MS/s in a double data rate for the reference generation time of $\tau_{\mathrm{clk}} = 600\,\mathrm{ps}$. The Walden FoM is evaluated to 97.8 fJ/conv-step.

Table I compares the post-layout prototype to single channel ADCs. In comparison to the conventional tracking ADC in [4], the proposed tracking ADC method provides a higher effective resolution and sampling rate. Compared to the state-of-the-art ADCs in 65 nm technology, the proposed design matches the SAR ADC in [8] and shows advantages regarding Walden FoM over the pipeline ADC in [9]. The enhanced sample rate due to technology scaling in [10] offers the possible performance increase by technology scaling.

V. Conclusion

A novel approach of extending the bandwidth limitations of tracking ADCs is presented. It generates a reference signal based on faster update rate than a conventional tracking ADC. In this way, this approach offers the tracking mode of higher input signal slopes compared to the conventional approach where the reference generation speed is limited by the total feedback-system delay. The derivation of two equations allows to determine the charactersistics to extend the bandwidth of the tracking ADC. The system concept provides self-adaption to system nonlinearity and offset. In comparison to the state-of-the-art, the proposed design provides performance parameters that are in the range of SAR or pipeline ADCs. The ability to scale down to technology nodes below the examined 65 nm, and thus to improve speed, resolution and power consumption, is indicated by the 94% digital implementation and by the correction system which compensates the comparator nonlinearity.

TABLE I
Comparison with a conventional tracking ADC, common ADC architectures in 65 nm technology and outlook for improved performance by technology scaling to 40nm.

	This Work	ISCAS' 13 [4]	ISSCC' 11 [8]	ISSCC' 15 [9]	ISSCC' 16 [10]
Architecture	**Tracking**	Tracking	SAR	Pipeline	SAR
Technology (nm)	**65**	130	65	65	40
Resolution (bit)	**8**	6	8	12	6
Sampling Rate (MS/s)	**323**	50	400	250	1000
SNDR (dB)	**40.65**	27.78	44.5	67	34.6
ENOB (bit)	**6.47**	4.33	7	10.83	5.4
Power (mW)	**2.8**	0.84	4	49.7	1.26
Active Area (mm^2)	**0.027**	0.08	0.024	0.59	0.00058
FoM (fJ/c.-s.)	**97.8**	83.5	73	126.8	28.7

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