Low phase noise, high resolution digitally-controlled ring oscillator operating at 2.2GHz

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Abstract—**A low power, high resolution, small area digitally-controlled oscillator (DCO) designed with TSMC 65nm CMOS technology is presented in this paper. The proposed design operates between the frequency range of 1.8 GHz and 2.2 GHz. The proposed system uses ring oscillator architecture with 4 stages of delay cell which is preferred due to its high stability and capability to operate with 6.10 kHz resolution. The active area of the DCO is 0.00037 mm^2 and power consumption varies between 0.6 mW and 1.6 mW for the supply voltage of 1.2 V. Monte Carlo simulation is performed, which gives a deviation of 7.4%, which proves the stability of the design.**

Index Terms—**Digitally-Controlled Oscillator(DCO), frequency generation, Digital to Analogue Converter(DAC).**

I. INTRODUCTION

In high-performance system on chip (SoC) providing applications like the Internet of Things (IoT) the multiple simultaneous frequencies are needed to connect to other devices in the network. These frequencies can be generated from phase-locked loops (PLL). It is a closed-loop system which uses phase locking architecture. PLL is widely used in radio, wired and wireless telecommunications, processors and other electronic applications [1].

The analogue PLL gives good resolution as well as phase noise performance with the cost of large chip size and high power consumption due to the analogue nature of loop filter. In contrast to an analogue PLL, digital PLLs consume less power and area while compromising the linearity, as the frequency can only be varied in finite steps determined by the resolution of the control bits [2]. The digital PLL needs less locking time and has a strong robustness against process, voltage and temperature (PVT) changes due to the lack of analogue components [3]. Accordingly, a digital PLLs has some disadvantages in terms of jitter and phase noise performance compared to an analogue PLL. In order to overcome
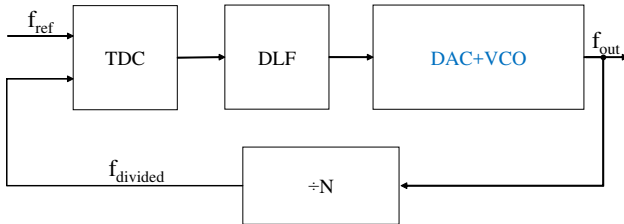

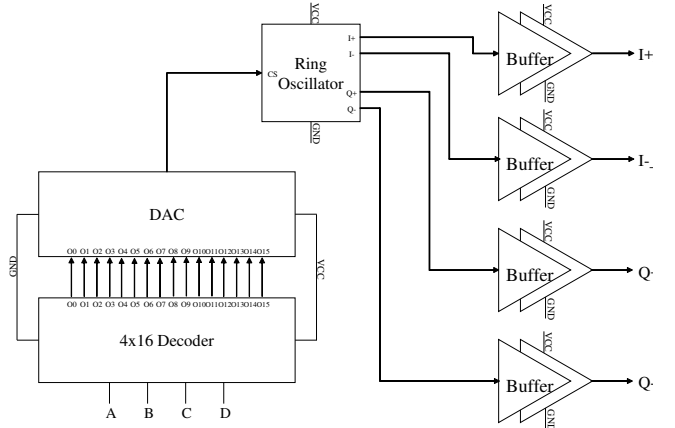Fig. 1: Block diagram of the proposed digital PLL.

Fig. 2: Block diagram of the proposed DCO.

these drawbacks, the proposed design consists of both voltage-control oscillator (VCO) whose control voltage adjusted by digital-to-analogue converter (DAC). In that way, while the advantages of VCO are retained in the system, power hungry and large sized blocks like loop filter can be eliminated.

The digital PLL is shown in Fig. 1, where the PFD is combined with Time-to-Digital Converter (TDC), which converts the phase difference to digital bits. This control word is then given digitally to the digital loop filter (DLF). Later, the digital signals from the DLF are used to control the VCO via the included DAC to reach the target frequency.

In the proposed work, the combination of DAC with its corresponding ring oscillator is proposed along with the output differential buffers. The conventional trade-off between the high resolution and wide frequency range tuning of such a DCO is reduced in the proposed design.

II. THE PROPOSED DESIGN

The proposed architecture of the DCO takes four control bits, as shown in Fig. 2, and controls the output frequency accordingly. The 4x16 decoder takes four control bits as the input for DCO. Alternatively, 16 control bits can also be directly given to the DCO, which increases the resolution of the DCO. These 16 control bits are taken as inputs to DAC, which controls the delay time of single cell by varying the current through the delay cell. The output stages of the oscillator should be capable to drive the following stages, and
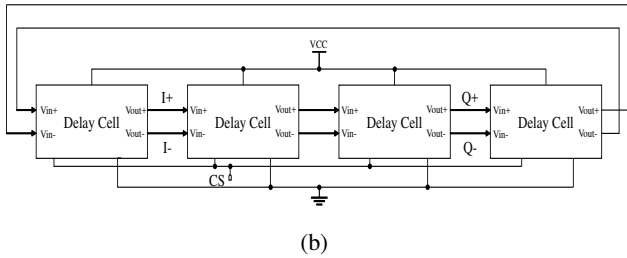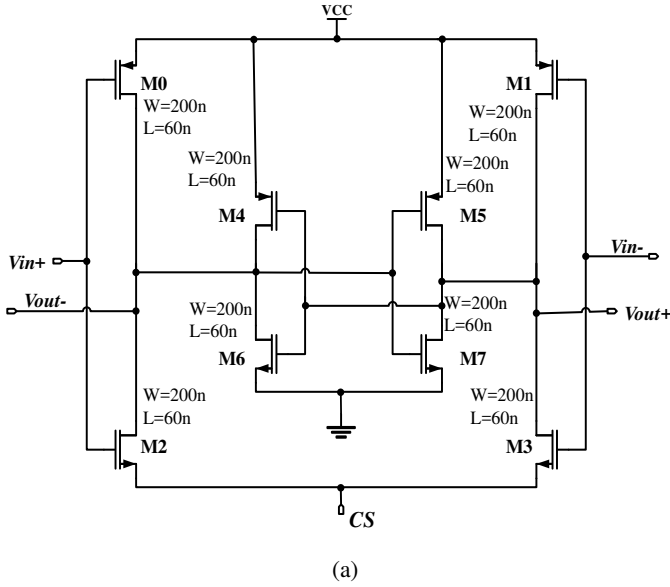
(a)

(b)

Fig. 4: (a)Schematic of delay cell, (b)Block diagram of the ring oscillator.

hence each of the output I+, I-, Q+, and Q- is fed to buffers. It is also taken care such that these buffers are strong enough to drive bigger transistors in the following stages.

A. DCO

The frequency tuning can be achieved digitally by two methods. The first method is to have different paths with various delays. The appropriate path is chosen with the help of a multiplexer, which leads to a change in oscillation frequency. The second method is to tune the delay in stages, which is achieved by introducing hysteresis delay cells or capacitors to the nodes, which both results in latch effects and changes the

frequency [4]. Alternatively, these delay stages can be varied by tuning the current at the charging and discharging nodes with the help of digital codes. The current sources occupy much smaller area and hence this approach leads to less power consumption, but the challenge is to guarantee a monotonic behaviour for the tuning ranges.

B. Delay cell

The proposed DCO is designed by using four delay cells, which are differentially controlled with the help of a Control Signal (CS) as shown in Fig. 4a. Delay cells with cross-coupled inverter architecture are chosen, as cross-coupling improves the phase noise and jitter performance. The bottom line of this structure is two driver inverters and two cross-coupled inverters. The delay results from the cross-coupled inverter which behaves like a latch. This delay is controlled by varying the node currents in the CS. The differential ring oscillator architecture is chosen due to its high stability, high efficiency, wide operating frequency range, and the ability to generate multi phase signals. The in-phase and quadrature signal components are obtained from the ring oscillator as shown in Fig. 4b.

C. DAC

The digital control signal for the delay cell is obtained from the unary-weighted transistor array as a current source as shown in Fig. 3. The proposed design has a resolution of 16 levels for linear and fine-tuning of the oscillator. To achieve linear voltage tuning, the pMOS is arranged in increasing order of the size from LSB, and the size of the $(n+1)^{th}$ pMOS is increased by a step of the smallest pMOS. The frequency of the oscillator increases as the size of the pMOS transistors increases as well as the current in the delay cell. The signal is obtained from the nMOS, which is always ON, hence the output capacitance is independent of the weighted pMOS, this makes the DCO linear. When using the DAC with the decoder, each pMOS in the DAC can be independently designed as only one pMOS will be active for a given time. This also gives the flexibility to assign the custom frequencies to the digital code words by tuning the pMOS size[5].

The 16 control bits for the DAC are obtained directly from the DLF or from the 4x16 decoder. When the control bits are provided directly to the DAC, the resolution of the DCO increases to $6.10\,\text{kHz}$. The decoder is the combinational circuit with N coded inputs and 2^N coded outputs. Every coded input
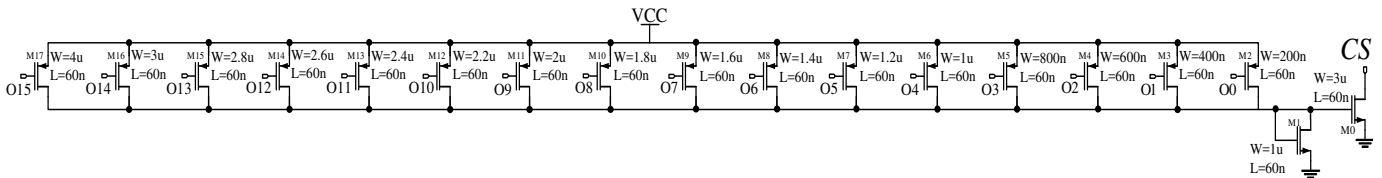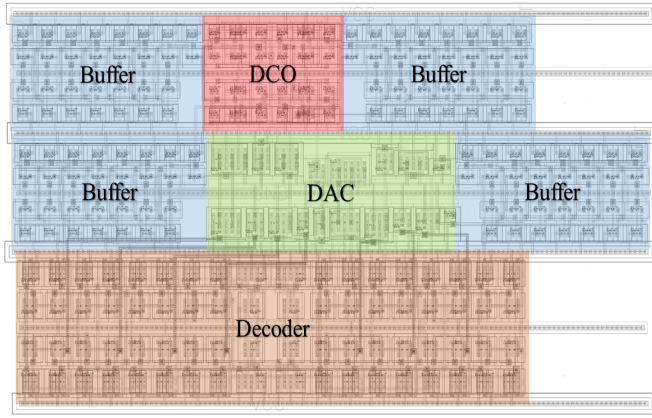

Fig. 3: Schematic of the proposed DAC.

Fig. 5: Layout of the proposed DCO.

signal has a set of unique output signals. It is achieved with the help of 16 AND gates and 4 inverters in this design. The 4 input signals <A,B,C,D> are obtained from the controller by comparing the reference signal and the divided output signal of DCO via the loop filter. In the proposed design, AND gates are replaced with NAND gates, as the pMOS is turned ON with logic LOW signal and turned OFF with logic HIGH. And also, a buffer with the same delay time as the inverter is used to equalise the signal delay introduced by the inverters.

III. LAYOUT AND SIMULATION RESULTS

The layout of the proposed DCO occupies an area of $26.33\,\mu m \times 14.32\,\mu m$ in TSMC 65 nm CMOS technology. The layout is designed such that the output from the oscillator should be equal in length with the buffers to avoid any phase difference in the output. All the simulations are performed with the extracted parasitics from the layout shown in Fig. 5.

The transient analysis of the DCO from the buffer is shown in Fig. 6 after reaching its steady state. As observed, the output of the oscillator is stable and switches between 0 V and 1.2 V. The proposed DCO operates at 1.8 GHz with 0000 codeword and at 2.2 GHz with codeword 1111. The phase
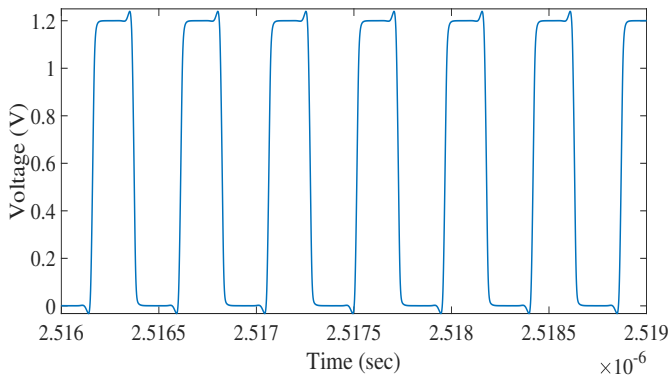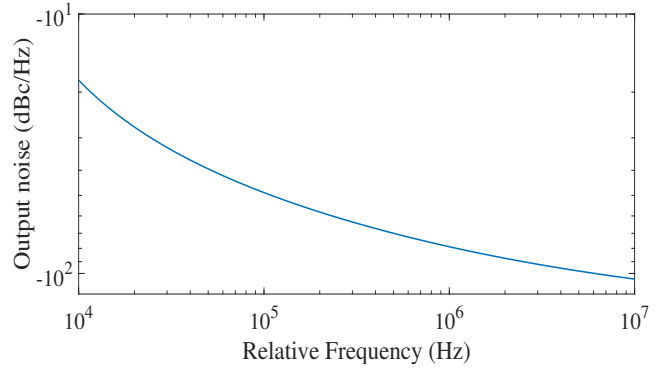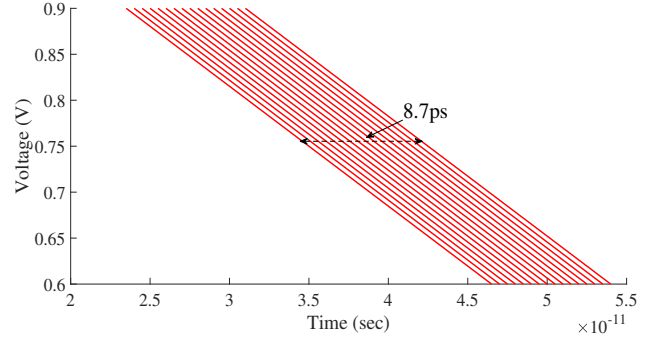

Fig. 6: Transient Simulation of DCO operating at 2.2 GHz.

(a)

(b)

Fig. 7: (a)Phase noise performance of DCO, (b)The peak-to-peak jitter performance of the DCO operating at 2.2 GHz.
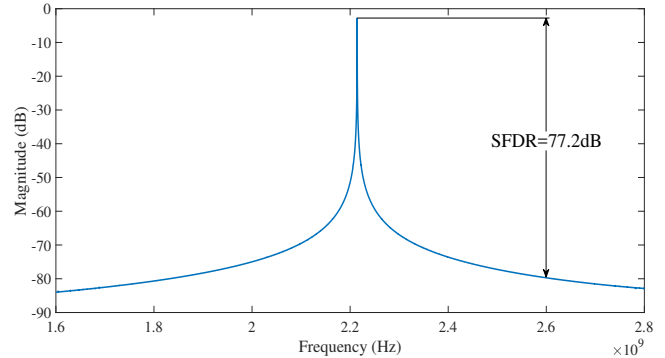

Fig. 8: Spectrum of the DCO operating at 2.2 GHz.

noise performance of the DCO is shown in Fig. 7a. The phase noise performance is quite good for a ring oscillator based DCO. In the closed loop system, better phase noise performance can be achieved with proper loop filter adjustment. This is often observed to measure the frequency fluctuations of the signal. The timing jitter performance of the DCO can be measured with the help of an eye diagram as seen in Fig. 7b. As observed, the peak-to-peak jitter at 2.2 GHz is 8.7 ps. The spectrum of a signal is often observed to measure the distortion of the desired signal by several other noise sources as shown in Fig. 8. The Spurious Free Dynamic Range

TABLE I: Performance Summary and comparison with state of art.

	This work	[5]	[6][1]	[7]	[8]
Technology (nm)	65	65	28	180	55
Tuning Range (MHz)	400	1900	730	800	2450
Phase Noise (dBc/Hz)	−78.9 @1 MHz	-	−109.5 @1 MHz	-	-
Peak-to-Peak Jitter (ps)	8.7 @2.2 GHz	6.47 @2.7 GHz	-	22.3 @1.28 GHz	9.6 @2.7 GHz
Resolution (kHz)	6.10	1500	-	1	-
VDD (V)	1.2	1.2	0.8	1.8	-
Power (mW)	1.6 [2]	1	0.35	22.68	1.103
Active Area (mm^2)	0.00037	-	0.042	0.053	0.0129
Figure of Merit[3](FOM) (dB)	-219.2	-223.8	-	-199.5	-220

[1] LC Tank based DCO

[2] It is the total power consumed by ring oscillator, DAC, Decoder and buffers.

[3] $\text{FOM}_{\text{jitter}} = 10 log_{10}\{(\frac{\sigma^2}{1\,\text{s}})(\frac{\text{P}_{\text{DC}}}{1\,\text{mW}})\}$

(SFDR) of the system is observed to be $77.2\,\text{dB}$ within almost $1.2\,\text{GHz}$ bandwidth. The proposed design gives a frequency resolution of $6.10\,\text{kHz}$. The power consumed by the proposed DCO at $1.8\,\text{GHz}$ is $0.6\,\text{mW}$ and at $2.2\,\text{GHz}$ is $1.6\,\text{mW}$. The proposed design outperforms state-of-art designs in terms of area, resolution, and power consumption as shown in TABLE I. As observed, the Figure Of Merit (FOM) of the proposed design outperforms [7] and is almost the same with [8]. Although [5] has better FOM, this work provides much better resolution. The DCO is also verified for its linearity without using the decoder, that is by giving 16 bit codewords directly to the DAC.

IV. Conclusion

A new approach for Digital-to-Analog Converter is proposed and validated in TSMC $65\,\text{nm}$ CMOS technology. Also, a 16-bit controlled Digitally Controlled Oscillator is developed with four stages of differential cells that can tune from $1.8\,\text{GHz}$ to $2.2\,\text{GHz}$. The design is checked for its phase noise performance, peak distortions and the jitter effects by plotting eye diagram. The layout of the proposed design has been generated, verified with DRC and LVS, and the parasitic components of the layout version are extracted. The proposed DCO is small in size, and has a good resolution with linearly increasing finite steps.

V. Acknowledgement

References

[1] Antonio Alvarez, *BiCMOS Technology and Applications,* Springer US, 1993.

[2] Behzad Razavi, *Design of Analog CMOS Integrated Circuit Design,* Mc-Graw Hill, 2001

[3] Abhishek Godave, Pranali Choudhari and Anita Jadhav, *Comparison and Simulation of Analog and Digital Phase Locked Loop,* 2018 9th International Conference on Computing, Communication and Networking Technologies (ICCCNT), July 2018.

[4] Macera Giuseppe, *Comparison of Voltage-Controlled Oscillator Architectures for implementation in 180nm SiGe Technology,* December 2016.

[5] J. Gorgi and M. B. Ghaznavi-Ghoushchi, *A 2.7 to 4.6 GHz Multi-Phase High Resolution and Wide Tuning Range Digitally-Controlled Oscillator in CMOS 65nm,* 24th Iranian Conferenece on Electrical Engineering (ICEE), May 2016.

[6] Run Levinger, Roi Levi, Evgeny Shumaker, Shunit Levin, Gil Horovitz, *A 3.9-4.7 GHz 0.35 mW DCO with -187.4 dBc FoM in 28nm CMOS,* 2018 13th European Microwave Integrated Circuits Conference (EuMIC), Sept. 2018.

[7] Xiaoying Deng, Yanyan Mo, Xin Lin, Mingcheng Zhu, *A 0.68-to-1.44 GHz low-jitter all-digital phase-locked loop with a novel PFD and a high resolution DCO in 0.m CMOS,* 2016 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Aug. 2016.

[8] Zhihong Luo, Guoxing Wang, Khalil Yousef, Benjamin Lau, Yong Lian, Chun-Huat Heng, *A 0.0129 mm2DPLL With 1.6 2.0 ps RMS Period Jitter and 0.25-to-2.7 GHz Tunable DCO Frequency Range in 55-nm CMOS,* IEEE Transactions on Circuits and Systems II: Express Briefs, Oct. 2018.