FPGA Implementation of High-Speed Data Acquisition System for High-Resolution Millimeter Wave Radar

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***Abstract*—This paper introduces FPGA implementation of high-speed data acquisition system for high-resolution millimeter wave radar. The transfer bandwidth of the Low Voltage Differential Signaling (LVDS) interface of the high-speed data acquisition system is 7200Mbps, which supports the cascade of four millimeter-wave radar sensors. The maximum transfer bandwidth of the DDR3 interface in the system is 12800Mbps, which is able to support high-bandwidth sample data storage of twelve millimeter-wave radar sensors. The maximum transfer bandwidth of Gigabit Ethernet interface in the system is 1000Mbps, which can adjust the transfer rate according to the system requirements, with good scalability. By using the high-speed data acquisition system designed in the article for the cascade of four high resolution 77GHz FMCW millimeter wave radar sensors , the system can achieve imaging with angular resolution close to 1.3 degrees.**

Keywords—FPGA, LVDS, DDR3 interface, Gigabit Ethernet, UDP

I. INTRODUCTION

Frequency Modulated Continuous Wave (FMCW) millimeter-wave radar can not only detect the presence of objects, but also detect the distance, speed and angle of the objects. However, it has been hindered in market applications such as intelligent driving [1] and the Industrial Internet of Things due to its low angular resolution for imaging. In order to overcome this challenge, Texas Instruments (TI) developed a series of single-chip 77GHz FMCW millimeter-wave radar data acquisition systems [2] . However, the transfer bandwidth of these hardware systems can not meet the requirements of high resolution imaging. The Field Programmable Gate Array (FPGA) not only has great transfer bandwidth, but also has the inherent ability to process and transfer large amounts of data in parallel [3]. It could be therefore used as an acceleration device to improve angular resolution of the data acquisition system for 77GHz FMCW millimeter-wave radar. An example of using FPGA to improve the transfer bandwidth and angular resolution of the system is shown in [4] for the implementation of LVDS interface, which avoids complex hardware design by utilizing the large number of differential IO pins on the FPGA to directly process high-speed multi-channel LVDS data in parallel, and it is therefore possible to cascade multiple radar sensors. By using Verilog HDL programming language and the IP core Memory Interface Generator (MIG) provided by Xilinx to design user interface [5], the DDR3 interface of the system developed in this article can improve the average reading and writing rate for bulk data storage, making the operation of SDRAM memory more simple. The Gigabit Ethernet interface proposed in the article realizes high-speed data transfer without occupying a lot of hardware resources. By employing the advantages of these high-speed interfaces, the high-speed data acquisition system based on FPGA for the cascade of four 77GHz FMCW millimeter-wave radar sensors is implemented.

The paper is structured as follows: in section II, we give the system architecture and system parameters. In section III, we present the system hardware platform and software implementation process. In section IV, we test and analyze the system performance. Finally, section V concludes the paper.

II. DESIGN

A. System Architecture

Fig.1 shows the proposed system framework, which gives the main design modules and data flow. Four radar sensors are integrated on the radar board, each of which supports four receiving antennas and three transmitting antennas [2]. On the KC705 development board kit, a Micron's MT8JTF12864HZ SDRAM chip is used to cache sample data of radar sensors, a Marvel's M88E1111 physical layer chip is used to transfer data from Gigabit Media Independent Interface (GMII) to the computer, and a XC7K325TFFG900-C FPGA chip is used as a control center for radar data flow [6]. The LVDS_DATA_-RECEIVER in FPGA mainly completes the collection and processing of multiple LVDS signals; the DDR3_CONTRO-LLER module mainly caches sample data; and the ETHERN-ET_CONTROLLER module mainly transfers Ethernet packets to the computer via Gigabit Ethernet interface.

B. System Parameter

In order to obtain the high angular resolution for imaging, the cascade of four FMCW millimeter-wave radar sensors is used. Each chip outputs a 300MHz clock signal and six channels of data signals. The format of output data of radar sensor is shown in the Fig. 2, where T_{IQ} is the time taken by a sample data; T_{samples} is the time taken by a frame of sample data; $T_{\text{idle\_time}}$ is the time interval between each frame of data.

a) LVDS bus transfer bandwidth: the theoretical transfer bandwidth of the LVDS bus in the system is given by

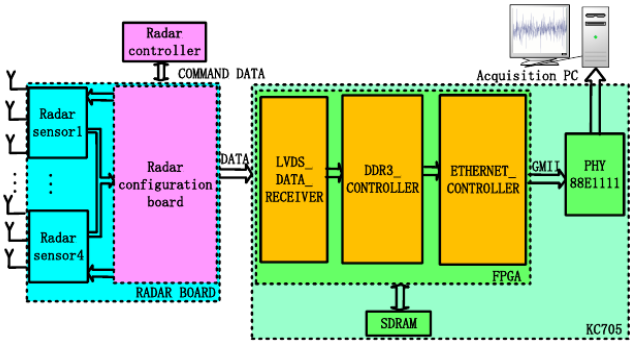


Fig. 1 Detailed acquisition system block diagram

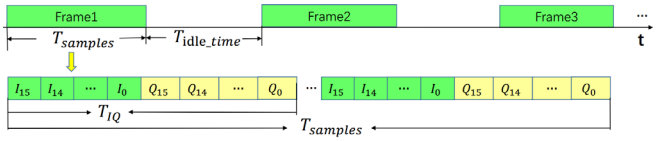


Fig. 2 Sample data format of LVDS bus.

$$V = N \times M \times f_{clk} \quad (1)$$

where M is the number of data channels for each radar sensor, N is the number of radar sensors, f_{clk} is the synchronous clock frequency of data signals. So the V is equal to7200Mbps .

Due to the gap between each frame of data, the effective transfer bandwidth of the LVDS bus is not equal to the theoretical transfer bandwidth and is given by

$$B = V \times \frac{T_{samples}}{T_{samples}+T_{idle\_time}} \quad (2)$$

where the T_{idle_time} is approximately 30us, and the $T_{samples}$ is close to 27.3us. So the B is about 3431Mbps.

b) Maximum transfer bandwidth of DDR3 interface: the SDRAM chip in the system supports DDR3 interface, and the transfer bandwidth of SDRAM is expressed as

$$B_{sdram} = f_{sdram\_clk} \times W_{bus\_width} \times \delta \quad (3)$$

where f_{sdram_clk} is the core frequency of the SDRAM memory and ; $W_{bus_width}$is bit width of memory bus; δ is the multiplication factor. In the system, the above three parameters are equal to 200MHz, 8 bits and 8, respectively. The maximum transfer bandwidth of DDR3 SDRAM is the equal to 12800Mbps [7]. According to (1) and (2), the DDR3 interface in the system supports high-bandwidth data storage of twelve radar sensors, which fully meets the requirement of system.

c) Ethernet interface transfer rate: in order to obtain more target information, the system needs to collect multiple frames of sample data at one time. The capacity of data that the system needs to store is

$$C = F \times K \times W_{sample\_width} \quad (4)$$

where F is the number of frames stored at one time, and K is the number of sample data in a frame, W_{sample_width} is the bit width of a sample data. The F, K and W_{sample_width} in the system are equal to 49152, 256 and 32 bits wide, respectively. The required C is then equal to 48MB and is fully satisfied by the capacity of SDRAM chip in the system, which is 1GB.

Considering that the system requires online processing and the transfer delay should not exceed 1s, the Gigabit Ethernet transfer rate is shown as

$$V_{eth} = \frac{C}{T_{delay}} \quad (5)$$

where T_{delay} is the maximum transfer delay allowed by the system.

According to (4) and (5), the required minimum transfer rate is 384Mbps, which is smaller than the maximum transfer rate of Gigabit Ethernet.

III. IMPLEMENTATION

A. Hardware

Fig. 3 shows the overall hardware physical map of the system. There are four cascaded radar sensors on the radar board to detect targets. And there is a KC705 development board kit officially launched by Xilinx to achieve the high-speed data acquisition. On the KC705 development board, there is a Gigabit Ethernet interface and SDRAM memory chip, and two FPGA mezzanine card (FMC) interfaces that support transfer of 92 LVDS signals. The FPGA acts as a control center to collect and process LVDS signals through FMC interface. The SDRAM chip caches high-speed data transferred by the LVDS interface of system. The Gigabit Ethernet interface transfers the data stored in the SDRAM chip to computer for processing through Gigabit Ethernet physical layer chip M88E1111 and RJ45 interface [8].

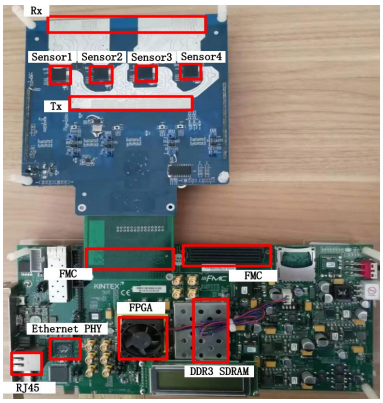


Fig. 3 Physical picture of system hardware.

B. Software

a) LVDS_DATA_RECEIVER module: as shown in Fig. 4, there are three clock signals in the LVDS_DATA_RECEIVER module. The 200MHz differential clock is generated by external crystal. The 300MHz clock and 200MHz ui_clk clock are both generated by the 200MHz differential clock. The clock signals have different roles, the 300MHz clock serves as the synchronous clock of the data_sync module, and the 200MHz ui_clk signal serves as the synchronous clock of the data_conversion module. The lvds_rx_data in the LVDS_DATA_RECEIVER module is responsible for receiving the LVDS signals and converting them to single-ended signals. The four data_sync modules use asynchronous First-In First-Out (FIFO) to perform cross-clock domain processing on the data output by lvds_rx_data module. In order to meet the requirements of DDR3_CONTROLLER for data bit width and the synchronization of sample data with the ui_clk clock, the data_conversion module performs bit-width conversion and cross-clock domain processing for data output by data_sync module, which facilitates data transfer between LVDS_DATA_RECEIVER and DDR3_CONTROLLER.

b) DDR3_CONTROLLER module: the overall architecture of DDR3_CONTROLLER is shown in Fig. 5. In the system, the capacity of SDRAM chip is 1GB, which consists of 8 pieces of 128MB memory and is controlled by 28 address lines [7]. With user_data_wr module, user_data_rd module,

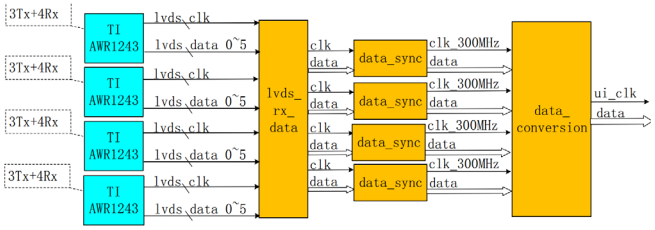


Fig. 4 Detailed LVDS receiver block diagram.

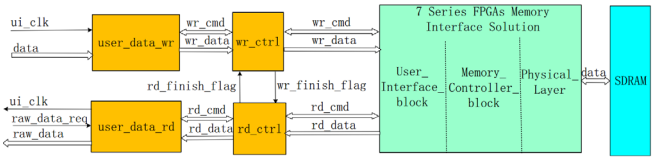


Fig. 5 Detailed DDR3 controller block diagram.

wr_ctrl module and rd_ctrl module designed in the paper, the *IP core* MIG can read and write data stored in the SDRAM chip quickly and efficiently.

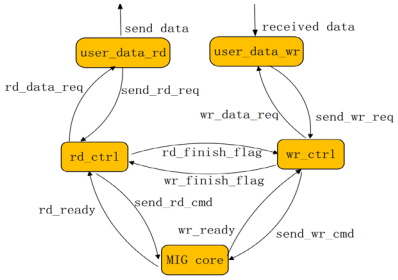


Fig. 6 Control process of DDR3 controller.

In the DDR3_CONTROLLER, the user_data_wr module consists of a synchronous FIFO that can store one frame of sample data, and the synchronous FIFO is used to receive the sample data from the LVDS_DATA_RECEIVER module. The user_data_rd module also consists of a synchronous FIFO that can store one frame of sample data, and the synchronous FIFO is used to receive the data from the SDRAM chip. Fig. 6 shows the control process of wr_ctrl module and rd_ctrl module with other modules, facilitating reading and writing data stored in the SDRAM chip.

c) ETHERNET_CONTROLLER module : Fig. 7 shows the design architecture of the ETHERNET_CONTROLLER module. Compared with TCP, the UDP protocol does not require a connection to be established before transmitting data, reducing the overhead and delay, so the UDP protocol is adopted to communicate with the computer. In the process of data transfer, the PHY 88E1111 chip can adaptively adjust the transfer rate. When the PHY 88E1111 chip operates at a Gigabit network operation mode, the clock frequency of the GMII port is required to be 125MHz and it is generated by the internal 200MHz clock.

In the ETHERNET_CONTROLLER module, the tx_data module performs cross-clock processing on data from DDR3 interface. In the process of Ethernet data transfer, a frame of sample data is transferred by ip_send_module, tx_data module send a raw_data_req signal to command user_data_rd module to update the data in synchronous FIFO. The ip_send-module refers to the IEEE802.3 standard and the UDP protocol to encapsulate the sample data into Ethernet data packets, and transfers the Ethernet data packets to the computer for processing through the physical layer chip M88E1111. The crc_module mainly completes the cyclic redundancy check on the data in the ip_send_module and sends the cyclic redundancy check results to computer.

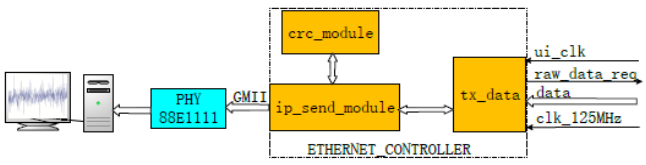


Fig. 7 Detailed Ethernet controller block diagram.

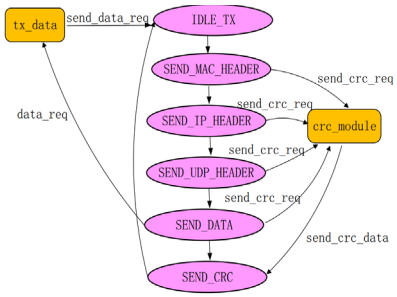


Fig. 8 Detailed data encapsulation process.

The data encapsulation process of the ip-send-module is shown in Fig. 8. There are six stages from IDLE_TX to SEND_CRC, and the tx_data module controls the beginning of packet encapsulation. The crc_module is responsible for cyclic redundancy check on the data in different stages to achieve the correct transfer of Ethernet data packets.

IV. RESULTS

In order to prove that the high-speed data acquisition system designed in this paper was successfully applied to high-resolution millimeter-wave radar systems, two sets of experiments were conducted. The first set of experiments tested the data acquisition system of TI's single high-resolution 77Ghz FMCW millimeter-wave radar sensor. The second set of experiments tested the data acquisition system implemented in this paper of the cascade of four high-resolution 77Ghz FMCW millimeter-wave radar sensors.

A. Performance test of millimeter-wave radar data acquisition system

In the high-speed data acquisition system with the cascade of four high-resolution millimeter-wave radar, there are 88 virtual multiple-input multiple-output (MIMO) transverse antennas, so the highest angular resolution in the horizontal direction is close to 1.3 degrees. In order to compare the performance of the system designed in this paper with the system designed by TI, the test environment of the two sets of experiments are almost the same.

Fig. 9 shows the system test scenario. In the test scenario, in order to ensure that the angle between the object 1 and object 2 to the radar is close to 1.3 degrees, the radial distance of Object 1 and Object 2 from the radar is set to 3.18 m and the distance between the two objects is set to 7.2 cm. For position reference, the angle between the object 3 and object 1 to the radar is set to 27.2 degrees and the radial distance of Object 3 from the radar is set to 6.17 m.

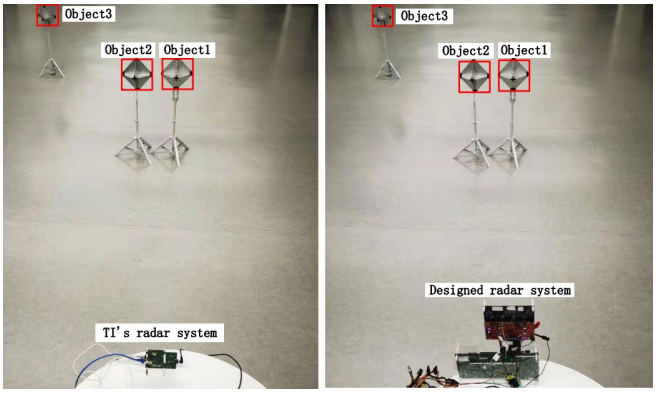


Fig. 9 Test of the system.

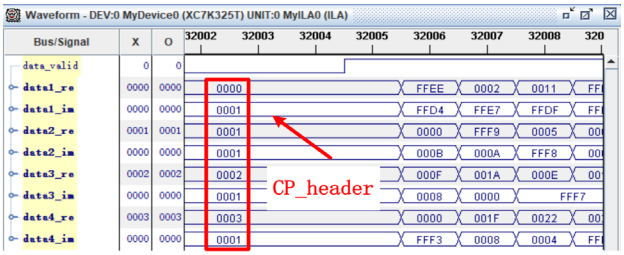


Fig.10 Test result of the LVDS interface.

B. *Test results and analysis of millimeter-wave radar data acquisition system*

The test results of high-speed interfaces designed in the paper are shown in Fig. 10 and Fig. 11. In the process of testing, the CP_header is added to each frame of sample data to test whether the data collected by the LVDS interface is correct; the installed network analysis software Wireshark is used to test and parse the Ethernet packets to evaluate whether the UDP protocol is correctly implemented and whether there are Ethernet data packet losses. The test results verify that the interfaces of system are correctly implemented.

In order to obtain high-resolution point cloud maps, the computer performs Fast Fourier Transform (FFT) and Constant False Alarm Rate (CFAR) algorithm on the data transferred by the high-speed interfaces. Fig. 12(a) shows the test results of TI's data acquisition system with single-chip millimeter-wave radar sensor and Fig. 12(b) shows the test results of data acquisition system with the cascade of four millimeter-wave radar sensors. Obviously, TI's data acquisition system with a single millimeter-wave radar sensor did not recognize Object 1 and Object 2, while the data acquisition system designed in the article identified two object ssuccessfully.

The TI's radar system cannot identify Object 1 and Object 2 owing to that it has only 8 virtual MIMO antennas in the horizontal direction, which results in the theoretical maximum angular resolution of approximately 14.3 degrees. Moreover, TI 's millimeter-wave radar data acquisition system can only support one chip to transfer data and cannot support more virtual MIMO antenna, which also limits the application of TI 's millimeter-wave radar system in high angular resolution. By contrast, the high-speed data acquisition system with the cascade of four millimeter-wave radar sensors developed in this work solves the problem well. It not only achieves higher angular resolution and supports multi-chip data transfer, but also improves flexibility.

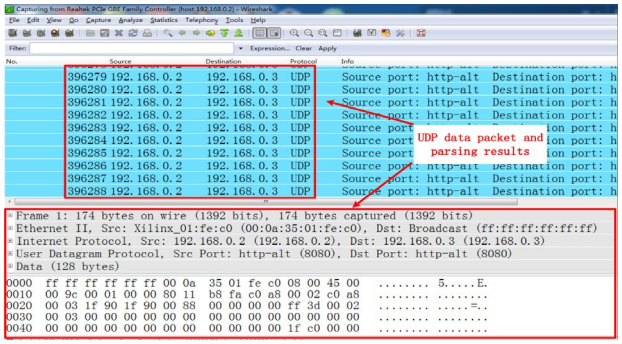
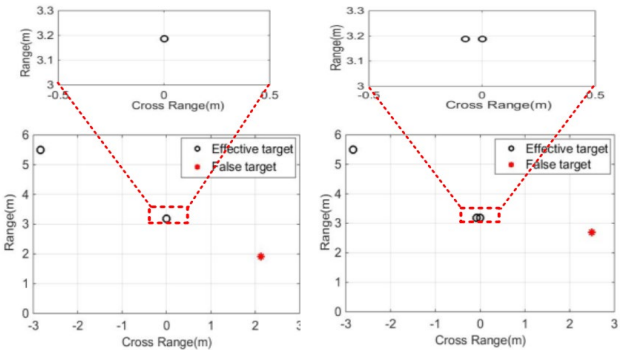


Fig.11 Test result of the Ethernet interface.



(a) (b)

Fig.12 Test results of the system.

V. CONCLUSION

A data acquisition system is proposed for 77GHz FMCW millimeter-wave radar in this work. As compared to the TI's data acquisition system used in its single-chip 77GHz millimeter-wave radar sensor AWR1243, the transfer bandwidth of LVDS interface is increased by three times to 7200Mbps, with improving the angular resolution from 15 degrees to 1.3 degrees; the maximum transfer bandwidth of DDR3 interface is increased by eleven times to 12800Mbps; the Ethernet controller module programmed in Verilog HDL language in the system only consumes 1% of the available hardware resources, and achieves good scalability with capability of adjusting its transfer rate according to the system requirements. In view of the great flexibility, the proposed system could be extended to multi-sensor multi-channel high bandwidth bulk data acquisition field in the future.

ACKNOWLEDGMENT

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