A 10-MHz Current-mode Constant On-time Boost Converter with a Translinear Loop-based Current Sensor

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***Abstract*— DC-DC converters with a high switching frequency are very attractive when fast-response, and small-area are required. In this paper, a translinear loop (TLL)-based digitally controlled current sensor is proposed for boost converters with the switching frequency of 10 MHz. Compared to previous current sensors, the proposed circuit helps to minimize the sensing response time by removing a slow feedback loop. It also uses a digital control to get an accurate sensing waveform. In addition, a ripple-based constant on-time (COT) control helps to further reduce the load-transient response. The proposed boost converter has been fabricated in a 180-nm CMOS process with a total chip area of 1.28 mm × 1.18 mm. The maximum conversion efficiency of 93.3% has been achieved even at the 10-MHz switching frequency, and 3.5-μs transient response time is measured at 400 mA of a load current step.**

***Keywords*— DC-DC boost converter, high-switching frequency, current sensor, translinear loop, constant on-time.**

I. Introduction

The growth of Internet of Things (IoT) applications requires DC-DC converters to have a higher power conversion efficiency and even smaller PCB area with small form-factor off-chip components. Furthermore, the trend of highly integrated system-on-chip (SoC) design leads the converters to have a much faster response against a large and fast load transient. Considering these harsh requirements, a high switching frequency operation with a realization of small off-chip components is desirable [1].

To achieve a fast-transient response, a ripple-based control method has been widely investigated [2]-[5]. This method does not limit either on-time or off-time of the converter, which helps to deliver an input power to an output in the fastest way. The ripple-based control in boost converters should use an inductor current waveform, since the output voltage is out of phase to the inductor current [6]. Therefore, a fast response current sensor design is very challenging for boost converters with the high switching frequency.

Previous current sensors usually rely on an analog feedback loop as shown in Fig. 1 [7]-[9]. The peak or valley of the inductor current are sensed by a replica sense-FET connected by a feedback error amplifier (EA). However, these current sensing circuits must have a limited loop bandwidth, which is dominantly determined by an output impedance of the EA and gate capacitors (C_{GS} and C_{GD}) of a pass transistor (M_{P3}). Thus,

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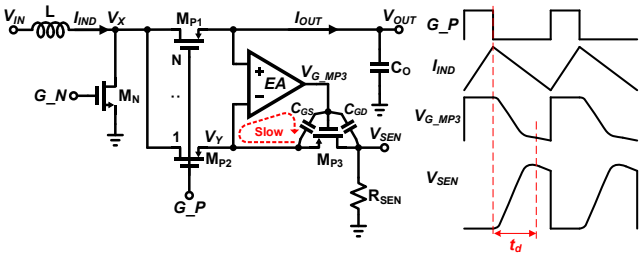
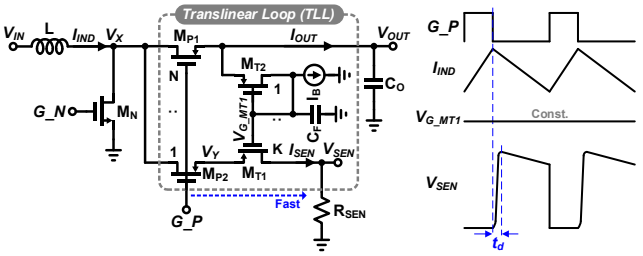
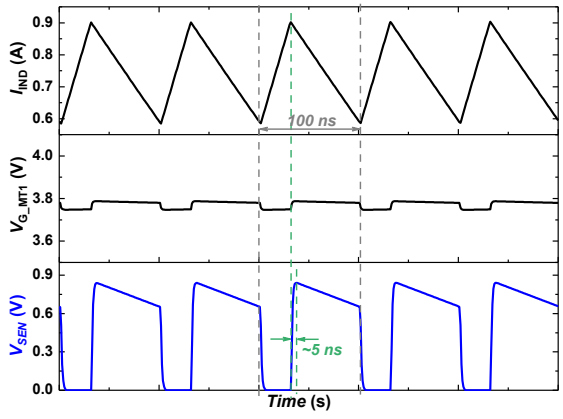


Fig. 1. Previous SenseFET-based valley current sensor [7]-[9].



(a)



(b)

Fig. 2. (a) Simplified circuit diagram of the proposed TLL-based current sensor. (b) Simulated waveforms of the proposed current sensor with the sensing response time.

it would limit a slew of gate voltage of M_{P3} (V_{G_MP3}) resulting in a slow response of the sensing output (i.e. tens of nanoseconds). This delay (t_d) from the sensing circuits would be very critical to the high-switching frequency applications over 10 MHz with only a hundred nanosecond of a switching period. Also, the excessive power consumption of the EA to achieve the faster sensing response results in the lower conversion efficiency. Thus, these schemes are not suitable for the high switching frequency applications. Another sensing scheme is a digital-based ripple injection current sensor [10]. The inductor current waveform can be emulated while an

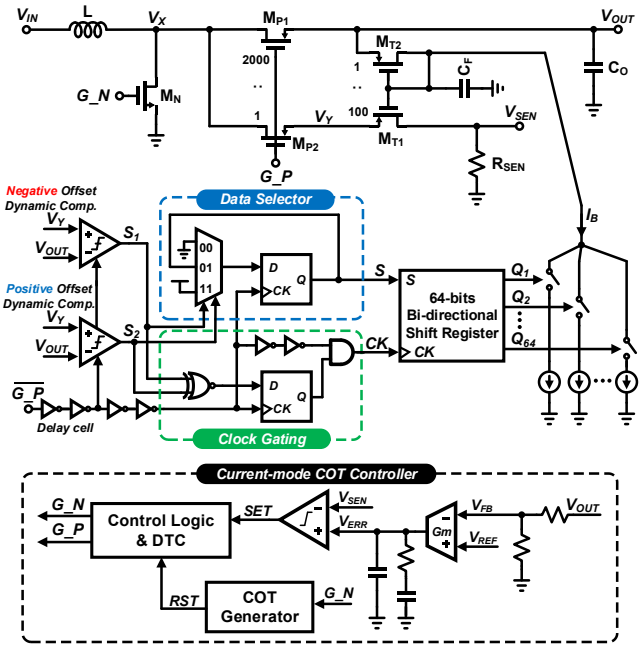


Fig. 3. Top block diagram of the proposed boost converter with the proposed TLL-based digitally controlled current sensor.

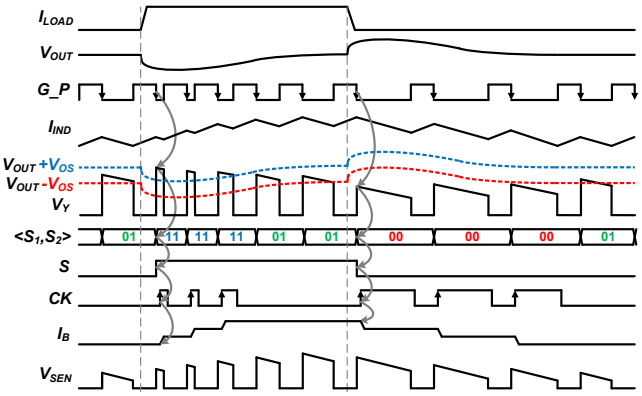


Fig. 4. Timing diagram of the load transient response with the proposed current sensor.

ADC senses input and output voltages to determine rising and falling slopes of the inductor current. This digital current sensor can achieve the fastest sensing response, which helps to realize the high switching frequency. However, the additional ADC requires a much faster extra sampling clock than the switching frequency.

In this paper, a translinear loop (TLL)-based digitally controlled current sensor is proposed to minimize the sensing response time. It also uses a digital control to get an accurate sensing waveform without any extra clock sources. The paper is organized as follows. The operational concept and circuit implementations of the proposed DC-DC boost converter are introduced in Section II. The experimental results are shown in Section III. And, Section IV concludes the paper.

II. Proposed TLL-based Current Sensor

Fig. 2(a) shows the simplified circuit diagram of the proposed TLL-based current sensor. A translinear loop (M_{P1}–M_{P2} and M_{T1}–M_{T2}) is implemented to sense an output current (I_{OUT}). If a bias current (I_B) is I_{OUT}/NK, the translinear loop will equalize V_{GS} of both M_{T1} and M_{T2}, resulting that a source voltage of M_{P2} (V_Y) equals an output voltage (V_{OUT}). That is, a sensing current (I_{SEN}) would approximate I_{OUT}/N, which is

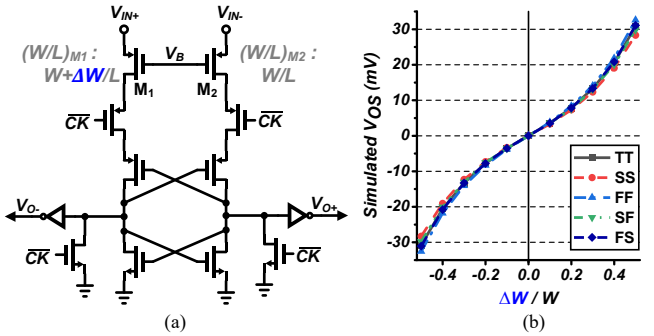


Fig. 5. (a) P-type common-gate dynamic comparator. (b) Simulated results of an input offset voltage (V_{OS}) with respect to the normalized input pair size mismatch.

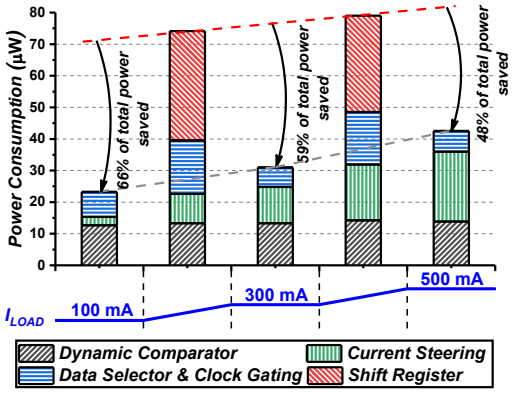


Fig. 6. Simulated power consumption of the proposed current sensor during the load transients.

the output current scaled down by a factor of N. Compared to previous feedback-based current sensors, only the feedforward path generates the sensing current. Therefore, the fastest current sensing is possible for the high switching frequency applications. Moreover, the power consumption can be saved by removing a power-consuming feedback amplifier. Fig. 2(b) shows the simulated waveform of a current sensing output (V_{SEN}) along with the inductor current (I_{IND}) under V_{IN} = 3.3 V, V_{OUT} = 4.5 V, and I_{LOAD} = 0.5 A, where V_{IN} is an input voltage and I_{LOAD} is a load current. Since M_{T2} is biased with a constant current of I_B, a gate voltage of M_{T1} (V_{G_MT1}) is nearly constant at V_{OUT}-V_{GS_MT2}. With this pre-defined gate voltage of M_{T1}, I_{SEN} can flow through M_{T1} immediately, resulting in 5-ns fast sensing response time of V_{SEN}. This delay can be considered reasonable for the 10-MHz high-switching frequency operations.

Since I_{OUT} is changed depending on the load current, I_B must be calibrated in accordance with changes to I_{OUT} in order to sense the accurate current waveform. If I_B is less than I_{OUT}/NK, V_{GS} of M_{T1} would be slightly larger than that of M_{T2}, resulting in V_{SEN} of significantly lower value rather than desired. In this paper, the digital control is used to calibrate I_B depending on variations to I_{OUT}. Fig. 3 shows a top block diagram of the proposed boost converter with the overall circuit implementation of the proposed digitally controlled current sensor. The digital control consists of two positive/negative-offset dynamic comparators, data selector, clock gating circuit, bi-directional shift register, and digitally controlled current steering array. Also, a capacitor (C_F) is used to reduce a switching noise from V_{OUT} and make a smooth transition to V_{GS} of M_{T2}.

At a falling edge of a PMOS gate signal (G_P), the two dynamic comparators directly monitor each source voltage of

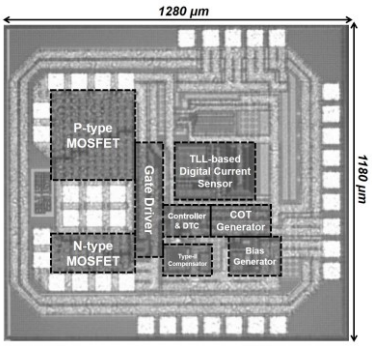


Fig. 7. Chip micrograph.

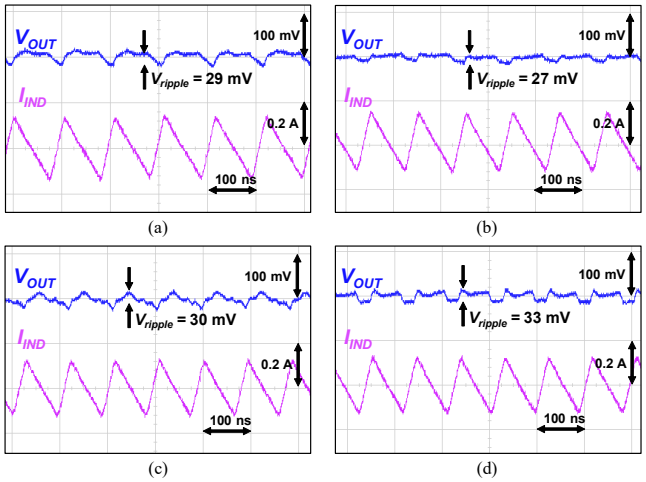


Fig. 8. Measured steady-state waveforms with (a) I_{LOAD} = 100 mA, (b) I_{LOAD} = 300 mA, (c) I_{LOAD} = 400 mA, (d) I_{LOAD} = 500 mA.

M_{P1}-M_{P2} (V_{OUT} and V_Y). Since each comparator has positive or negative input offsets in purpose, it makes two detection levels (V_{OUT}+V_{OS} and V_{OUT}-V_{OS}) to determine a status of the I_B. The data selector and clock gating circuit are implemented to reduce a power consumption of the 64-bits shift register when the converter operates in a steady-state. The data selector tries to maintain the output (S) with a previous value if the <S_1,S_2> becomes <0,1> at a next falling edge of the G_P. The transition of S is only happened when both S_1 and S_2 are identical. Also, the clock gating circuit blocks the clock signal (G_P) to the shift register if the S_1 and S_2 are nonidentical. Therefore, the input and clock signals (S and CK) of the 64-bits shift register can be blocked when the converter is in the steady-state.

Fig. 4 shows a timing diagram of the proposed current sensor during a load transient response. If the load current (I_{LOAD}) increases, I_B becomes insufficient to bias the translinear loop MOSFETs (M_{T1}–M_{T2}), resulting that V_Y is slightly larger than an upper detection level of the comparator (V_{OUT}+V_{OS}). Then, both S_1 and S_2 are changed to high signal, and the S and CK of the shift register are triggered to increase I_B through the digitally controlled current steering array. Subsequently, V_Y becomes within two detection levels of the comparator (V_{OUT}-V_{OS} and V_{OUT}+V_{OS}), and the CK is blocked to maintain the current status of I_B. Since most of power consumption in the digital logic is occurred in the 64-bits shift register, the significant power can be saved at the steady-state operation. When I_{LOAD} decreases, the control logic works to decrease I_B in a similar manner.

Since the dynamic comparator should directly compare the output voltage, a p-type common-gate dynamic comparator is proposed in Fig. 5(a). The gate of PMOS input pair (M_1-M_2)

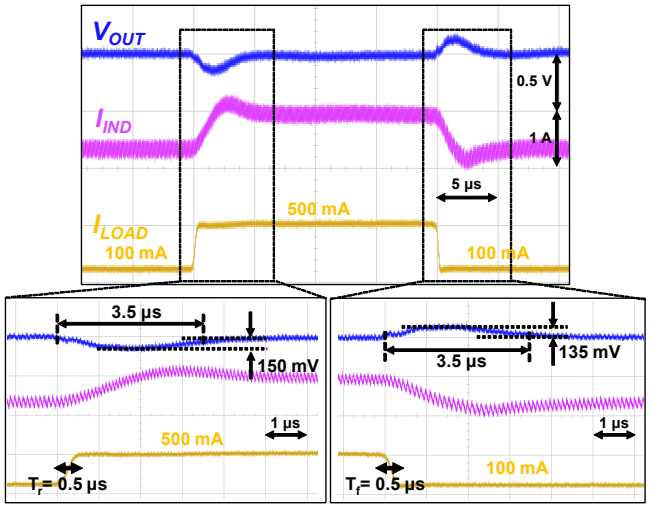


Fig 9. Measured load transient response when the load current steps from 100 mA to 500 mA.

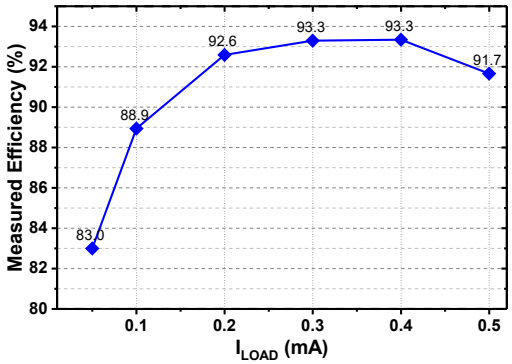


Fig 10. Measured conversion efficiency with respect to the load current.

is commonly connected to V_B, and their V_{GS} difference determines the outputs (V_{O+} and V_{O-}). Furthermore, the size mismatch of the input pair realizes the positive or negative input offsets. Fig. 5(b) shows a simulated input offset voltage (V_{OS}) under V_{OUT} = 4.5 V with respect to a normalized input pair mismatch. Even with variations of process corners, the desired offset voltage can be precisely obtained with the input pair mismatch.

Fig. 6 shows a simulated power consumption of the proposed current sensor during the load transients under V_{IN} = 3.3 V and V_{OUT} = 4.5 V. Depending on an increment of I_{LOAD}, a total power consumption has a tendency to be also increased since the current steering array will increase the amount of I_B. Compared to the transient of I_{LOAD}, the 64-bits shift register at the steady-state does not consume the power anymore, and the power consumption of the data selector and clock gating circuit can be also reduced by removing a unnecessary switching behavior to drive a huge input capacitance of the 64-bits shift register. Therefore, the power consumption under 50 μW at the steady-state can be achieved while saving the maximum 66% of the total power at I_{LOAD} = 100 mA.

III. Measurement Results

The proposed boost converter has been fabricated in a 180-nm CMOS process. Fig. 7 shows a chip micrograph with a total chip area of 1.28 mm × 1.18 mm including I/O pads and sealing. The off-chip inductor and output capacitor are 300 nH and 6.6 μF, respectively. The output capacitor is composed of three parallel of 2.2 μF to reduce an equivalent series inductance (ESL) of the output capacitor. Otherwise, the

TABLE I
COMPARISON TABLE OF THE PROPOSED BOOST CONVERTER TO THE PRIOR-ARTS BOOST CONVERTERS

Publications	[11] TPE '15	[12] TCAS-II '18	[6] TPE '15	[8] JSSC '18	**This Work**
Control Method	Current-mode Constant Off-Time	Constant Peak-Current	Voltage-mode Constant On-Time	Current-mode Constant On-Time	**Current-mode Constant On-Time**
Technology	0.5-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	**0.18-μm CMOS**
Input Voltage (V)	5	1.2	0.22 – 1.3	0.8 – 1.4	**3.3**
Output Voltage (V)	5.5 – 36	1.8	1.8	1.8	**4.5**
Max. Load Current (mA)	500	50	50	400	**500**
L (μH)	3.3	10	N/A	1	**0.3**
C_{OUT} (μF)	20	47	N/A	6.8	**6.6 (2.2 ×3)**
f_{SW}	1 MHz	Max. 40 kHz	Max. 93.8 kHz	0.8 MHz	**10 MHz**
Max. Efficiency (η_{PEAK})	92.94%	88.39%	90.6%	92.4%	**93.3%**
Die Size (mm²)	4	0.43	0.72	0.88	**1.51**
Load Transient	42 μs @150 mA → 350 mA	N/A	N/A	14 μs @10 mA → 400 mA	**3.5 μs @100 mA → 500 mA**
Recovery Time (T_R) / Load Current Step (I_{STEP})	0.21 μs/mA	N/A	N/A	0.036 μs/mA	**0.0088 μs/mA**
FOM	4.519	N/A	N/A	0.971	**0.188**

output voltage ripple could be degraded in the high switching frequency.

The measured steady-state waveforms are shown in Fig. 8(a)-(d). The maximum output voltage ripple of 33 mV is measured under I_{LOAD} = 0.5 A. Fig. 9 shows the measured load transient response with I_{LOAD} from 100 mA to 500 mA. With the load current steps of 0.5-μs transient time, undershoot and overshoot voltages of V_{OUT} are measured as 150 mV and 135 mV, respectively. Meanwhile, the fast recovery time of 3.5 μs is measured when the I_{LOAD} changes.

Fig. 10 shows the measured conversion efficiency as a function of I_{LOAD}. The maximum conversion efficiency of 93.3% is measured under I_{LOAD} = 300 mA and 400 mA. The comparison table compared to the prior-arts ripple-based boost converters is shown in Table I. The proposed converter is realized with the smallest form-factor off-chip components and achieves the maximum conversion efficiency of 93.3% even at the fastest switching frequency of 10 MHz. And, the fastest recovery time of 3.5 μs against 400 mA of the load current step and the state-of-the-arts recovery time per current step are achieved. A figure of merit (FOM) is defined to compare the performances as follows

$$\text{FOM} = \frac{T_R}{\eta_{PEAK} I_{STEP} I_{LOAD,\text{MAX}}} \qquad (1)$$

The smaller FOM stands for the faster transient response with the higher peak efficiency, and the proposed converter shows the better FOM compared to the prior-arts boost converters.

IV. CONCLUSION

This paper introduces the TLL-based digitally controlled current sensor for boost converters with the high switching frequency. Compared to previous feedback-based current sensors, the TLL-based current sensor helps to significantly reduce not only the sensing response time, but the power consumption. By implementing the digital control including the data selector and clock gating circuit, the translinear loop is calibrated without any extra clock source while minimizing the power consumption at the steady-state condition. The proposed boost converter has been fabricated in a 180-nm CMOS process. The load transient response time is measured at only 3.5 μs with the load current step from 100 mA to 500 mA. The maximum conversion efficiency of 93.3% has been measured.

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