A Two-Level, High Voltage Driver Circuit with Nanosecond Delay for Ultrasonic Transducers

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***Abstract*— In this paper, a two-level, high voltage (HV) driver circuit for driving ultrasonic transducers is presented. The circuit is specifically designed to drive a Capacitive Micromachined Ultrasonic Transducer (CMUT). The driver circuit has no static power consumption from the high voltage power rails which makes it suitable for low power portable ultrasonic applications. The HV driver has a measured peak to peak voltage swing of 47 V at 1.8 MHz pulse frequency. The rise and fall times of the pulses are 78 ns and 67 ns respectively. The work also demonstrates the possibility to have a fully integrated front-end solution for CMUTs without the need to use an external DC bias. The total layout area of the driver circuit is 0.22 mm^2. The presented circuit is fabricated using a 0.18 µm HV SOI CMOS process.**

Keywords— High Voltage analog front end, Driver circuit, Level Shifter, Ultrasonic Imaging circuits

I. INTRODUCTION

Ultrasound based sensing is a widely used technique for a range of applications. Some of the popular applications are medical imaging, material characterization and non-destructive testing, gesture control, automotive and robotic sensors. The non-ionizing nature of the ultrasonic sound waves makes it safe to be used on humans allowing it to be used for diagnostic and therapeutic applications. Traditionally, piezoelectric transducers are used at the scanning head of the ultrasonic probes. The advances in micromachining processes lead to the development of capacitive micromachined ultrasonic transducers (CMUT) [1] which allows fabrication of multi-array transducers in a small form factor. In addition, the CMUTs have wide bandwidth operation and compatibility with CMOS manufacturing process which allows for a monolithic integration with the analog front-end electronics.

CMUTs are micromachined structures with two membranes. One of the membranes is fixed and the other is movable. By placing a DC voltage across the membranes, a coloumbic force of attraction is produced which pulls the movable membrane. An alternating voltage superimposed over this will cause the membrane to deflect and generate ultrasound waves. When an ultrasonic wave impinges on the membrane, the deflection results in a current to flow due to change in capacitance of the CMUT. The same transducer device can be used as both transmitter and receiver in a time interleaved manner. Figure 1 shows a typical ultrasound transceiver channel of a front-end integrated circuit. In the transmit mode, a HV pulse generating driver circuit on the IC produces pulses which are AC coupled and applied to one of the electrodes.

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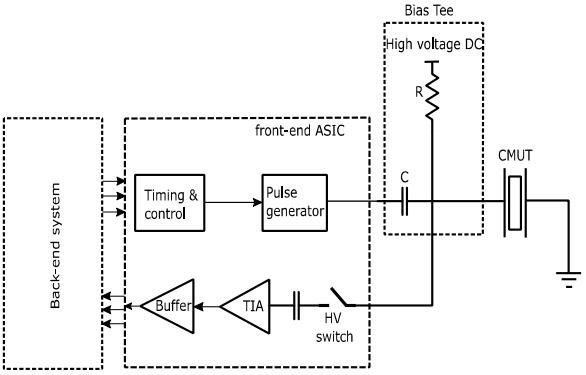

Fig. 1. A conventional CMUT transmit-receive chain

An external RC bias tee circuit will ensure that the CMUT is biased to a high DC voltage level. In order to ensure that the user is not exposed to high voltages, it is recommended to ground the top electrode. A HV protection switch will isolate the low voltage circuitry in the receive path. A close integration possibility of the CMUTs with the analog front-end electronics makes the CMUT based ultrasonic systems an attractive option for portable ultrasonic imaging or testing systems. This further makes it possible to lower long interconnect cables from the back-end system and also the signal to noise ratio can be improved if the received signals are amplified close to the transducer before sending it to the back-end signal processing unit

A single chip solution with monolithic integration of CMUT over CMOS or two chip solution where the ASIC and the CMUT chip integrated using flip chip bonding is a possibility [2]. Minimizing the off-chip components should be a priority for such closely integrated systems. In this work, we have presented a two-level HV driver circuit for the CMUT which allows us to avoid the use of the bulky external RC bias tee circuit. The driver circuit switches between two high voltage levels during the transmit mode. This is equivalent to applying a high DC bias and superimposing an AC pulse over it. During the receive mode, the output of the driver circuit is set to a high DC level so that the CMUT still has a high receive sensitivity as in the conventionally used architecture.

This paper is organized as follows. In section II, the challenges involved in designing a low power, highly integrated front-end with a conventional driver topology is explained. The proposed driver circuit is presented next with a short description of the circuit operation. In section III, the measurement results of the circuit are provided and a table of comparison with previous similar works are provided. This is followed by a conclusion in section IV.

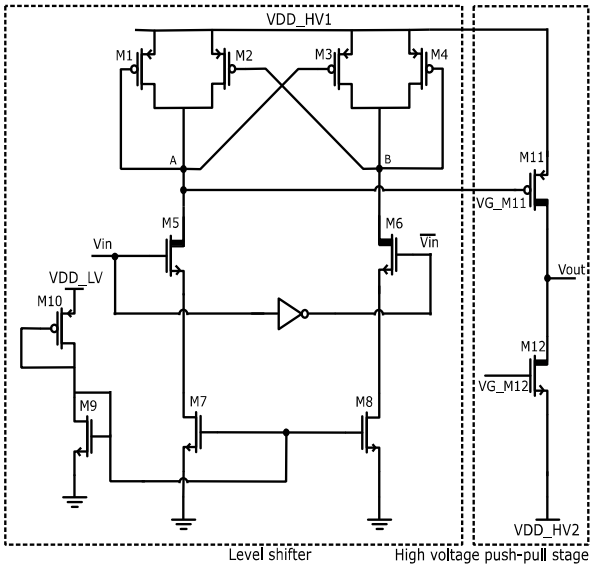

Fig 2: A current-limited static level-shifter based driver circuit.

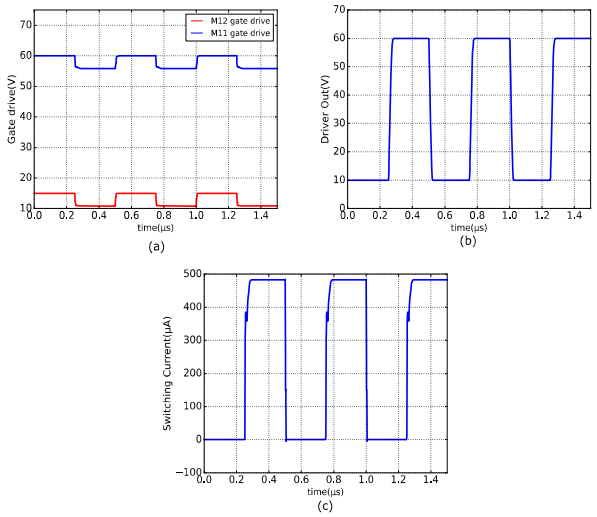

Fig. 3. (a) Gate drive signals (for M11 and M12) for the push-pull stage.
(b) Output voltage of the driver circuit.
(c) Current through transistor M7of level shifter.

II. HIGH VOLTAGE DRIVER CIRCUIT

A. *Standard circuit topology and Design Challenges*

To drive the ultrasonic transducers in the transmit mode, a HV driver circuit is required. HV transistors that are used for these designs have a high drain-source and drain-bulk voltages. However, the maximum gate-source voltage of such transistors is limited to standard digital logic voltage levels. For this work, we have used a process with $V_{DS\ (max)}$ of 200V and $V_{GS\ (max)}$ of 5 V. A HV driver circuit uses a level shifter [3] and an output push-pull stage to produce HV pulses. The level shifters used can be static or dynamic level shifters. In Fig. 2, a HV driver circuit based on static level shifter [4] is shown. The driver circuit uses only 4 HV transistors M5, M6, M11 and M12. For ease of identification, the HV transistors are drawn with a thicker drain terminal. The circuit is a slight modification of the one presented in [3] with a current limit circuit formed by M9, M7 and M8. By adjusting the aspect ratio of M10, the maximum current drawn from the HV supply (VDDH) to ground can be restricted. The low voltage control input is applied to M5 and M6. Nodes A and B are clamped to a safe limit using diode connected transistors M1 and M2. M11 and M12 form the push-pull stage of the driver.

For this work, the requirement is to design a driver circuit that switches between two HV levels (60V and 10V). This means that the low side NMOS transistor in the push-pull stage has its source connected to 10V. So, a level shifter is required to drive the low side transistor as well. A driver circuit is designed using the same level shifter architecture shown in Fig. 2 and the simulation results are shown in Fig. 3. As it can be seen, there is a current consumption of 493 μA for each half cycle through each of the level shifter branches from 60V. A same amount of current is drawn from the 10V supply as well. This accounts to an average power consumption of 35mW per driver. For systems with a large array of CMUT elements, such large power consumption could lead to a large power budget and heating issues. Hence, a low power, dynamic level shifter is designed to be used for the final system design.

B. *Low power dynamic level shifter based driver circuit*

To further lower the power consumption, a cross-coupled dynamic level shifter based on [5] is designed. The schematic of the proposed driver circuit is shown in Fig. 4. The circuit has no static power consumption and uses no HV capacitors. The design uses only 4 HV transistors. The transistors placed in the green dashed lines are low voltage (LV) transistors floating at a high voltage level. These are 5V transistors and hence care must be taken at all times to make sure that the voltage difference between various circuit nodes are within the maximum tolerable level.

We designed two identical level shifters to drive both the high side PMOS and low side NMOS of the push-pull stage. For simplicity and clarity of explanation, we will focus only on the high side level shifter. The low side level shifter follows an identical design and analysis. The VDDH and VSSH used for the design are 60 V and 56 V respectively to ensure that the floating LV transistors are in the safe limit. A high voltage linear regulator [6] with a high current capacity supplies the 56 V. So, the transistors M5 to M10 are placed in the same well that floats between 56V and 60V. The low voltage control signals are applied to the transistors M1 and M2. PMOS transistors M3 and M4 protects the floating LV transistors. M7 and M8 are used to pull down the sources of M3 and M4 to VSSH. M7 and M8 should be made much weaker than M5 and M6 to ensure that the latch changes its state. The circuit does not consume any static current. There is a current flow from the HV power supply to ground only when there is a switching activity happening. The sizing of the transistors is done as follows: Lets us assume initially that the node N_L2 is at VDDH and N_R2 at VSSH. To flip the state, we have to apply HIGH at gate of M1. At this stage, M1 pulls N_L1 to ground. M3 turns ON in saturation and pulls node N_L2 down. It should be pulled at least a Vthp below VDDH to flip the state. The ratio of M3 to M5 decides how fast node N_L2 is discharged. We can equate the currents of the two transistors to get:

$$\frac{(W/L)_3}{(W/L)_5} = \frac{2.Kp_5(VDDH-VSSH-Vth_5)Vth_6}{Kp_3(VDDH-Vth_6-VSSH-Vth_3)^2} \qquad (1)$$

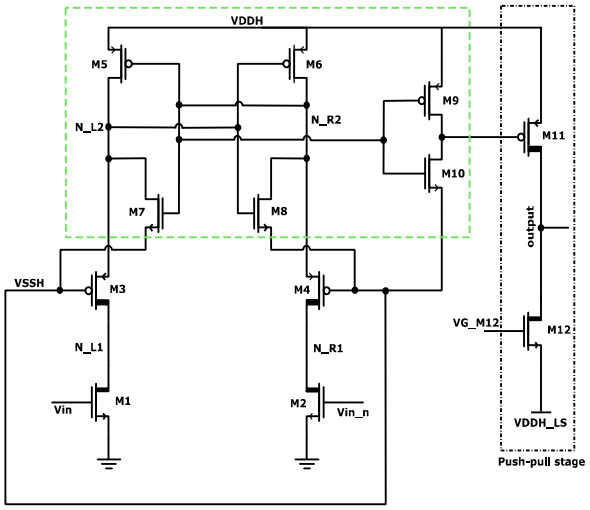

Fig. 4. A dynamic floating level shifter

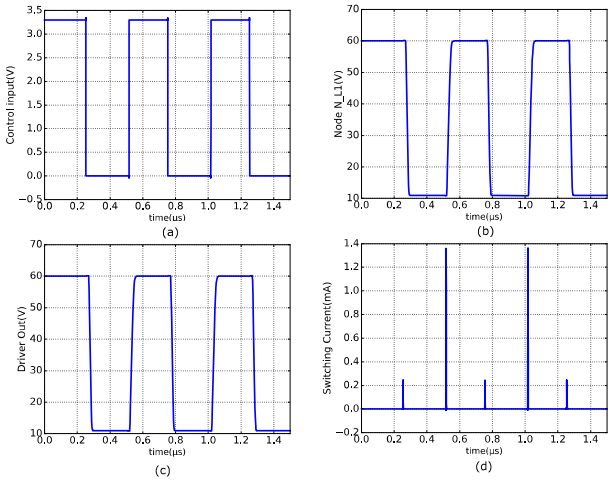

Fig. 5. Post-layout simulation results of the final driver circuit

In a similar way, M1 is sized relative to M5 to ensure sufficient current to flip the state of the latch. As for (1), we can derive a scaling factor of the aspect ratios of the M1 and M5 as:

$$\frac{(W/L)_1}{(W/L)_5} = \frac{2.Kp_5(VDDH-VSSH-Vth_5)Vth_6}{Kp_1(Vin-Vth_1)^2} \qquad (2)$$

The gate control for the low side NMOS transistor M12 of the push-pull stage is produced using the same level shifter architecture explained above. The post-layout simulation results of the final CMUT driver circuit are presented in Fig. 5. In 5(a) the low voltage input control signal is shown, in 5(b) the switching of the node N-L1. In Fig. 5(c), the output of the high voltage driver circuit is shown. The switching current of the transistor M1 is shown in 5(d). It can be seen that the maximum current during switching is 1.38 mA. This flows for a very short period of time of ~ 2.8 ns until the latch changes its state. This delay is mainly associated with the charging of capacitors at various nodes in the circuit.

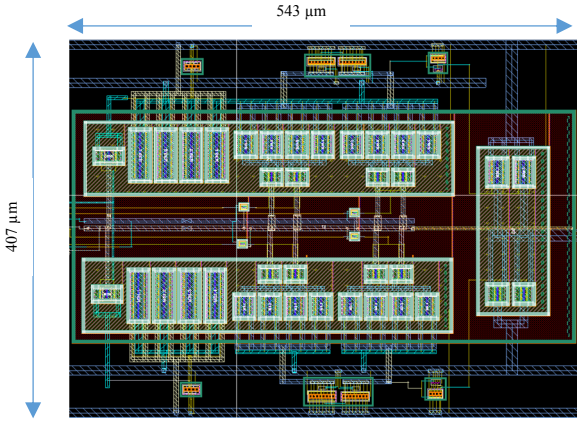

Fig. 6. Layout of the driver circuit

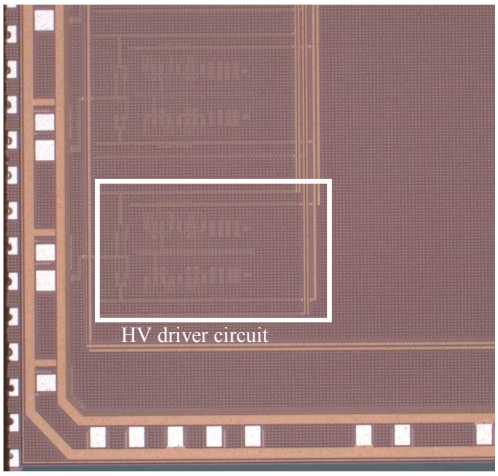

Fig. 7. Chip photograph of the driver circuit

III. Measurement Results

The design is fabricated in a 0.18µm HV SOI CMOS process. The key measurement results are presented in this section. In Fig. 6 and 7, the final layout and chip photographs of the circuit are shown. The test-chip is fabricated with 8 driver circuits in order to interface with a 2-D CMUT array. A test PCB was designed to characterize the chip. DC power supplies of 3.3V, 60 V and 15 V are provided externally. Two high voltage integrated linear regulators with high current sinking capability provide 56V and 11.5V for biasing the high voltage transistors in the level shifters. The 11.5V LDO also forms the lower side power rail for the push-pull driver stage. The HV driver circuit is characterized by applying a 3.3V square wave at 1.8 MHz using an external FPGA. To avoid conduction between the high voltage rails, a non-overlapping control signal generation circuit on the chip produces 4 control signals for the level shifters. The total output capacitance loading for the driver circuit is estimated to be around 15 pF which includes the probe capacitance and PCB pad and routing parasitic capacitances. In Table I the important circuit performance parameters are listed and compared with similar works. It can be seen that the presented work has the lowest current consumption with comparable rise and fall times. The input to output delay of 28 ns is one of the smallest. Only [7] has a better input-output delay, however this is for a 10 V pulse.

TABLE I

PERFORMANCE PARAMETERS OF THE IMPLEMENTED DRIVER CIRCUIT AND COMPARISON TO PREVIOUS WORKS

Parameter	This work	[7]	[8]	[9]	[10]
Peak to peak pulse voltage	47 V	9.8 V	15 V	59 V	30 V
Frequency	1.8 MHz	1.25 MHz	2.6 MHz	3.8 KHz	1.38 MHz
Output Load	15 pF	15 pF	12 pF	20 pF	18 pF
Input-output delay	28 ns	22.5 ns	30.8 ns	N.A	34 ns
Rise/fall time	78 /67 ns	40-50 ns	57/30 ns	69/60 ns	68/65 ns
Power consumption	1.38 mA dynamic	19.9 mA dynamic	N.A	120 mW static	98.1 mW
Chip area	0.22 mm^2	0.022 mm^2	0.15 mm^2	N.A	0.08 mm^2
Process technology	0.18 µm SOI CMOS	0.18 µm BCD	0.18 µm CMOS	0.8 µm CMOS	0.35 µm CMOS

IV. CONCLUSION

A two-level nanosecond-delay high voltage (HV) driver circuit for capacitive micromachined ultrasonic transducers (CMUT) is designed and implemented in a 0.18 µm HV SOI CMOS process. The measurement results show a close matching to the required system specifications to drive an array of CMUT transducers with a resonant frequency of 1.8 MHz. The design provides a low power, area efficient solution for close integration of CMUTs and front-end electronics ASIC.

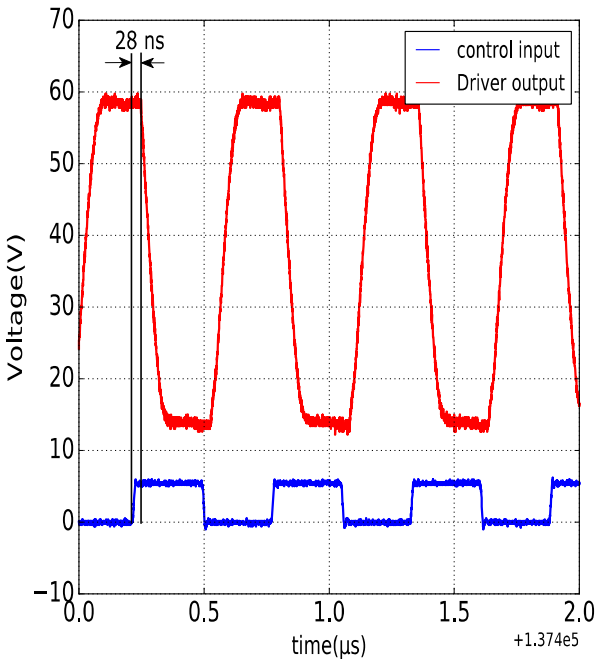

Fig. 8. Measurement result of the high voltage driver output

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