Applying the Power Contributors Method in a complex CMOS cell

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***Abstract*— The evaluation of a circuit library in terms of leakage currents and static power consumption is obligatory for low power designs. It has to be done early in the design process and it requires significant time effort. Both the leakage currents and the static power consumption depend on many parameters, such as: process, dimensions, temperature, cell's input state and power supply voltage. In order to speed up the evaluation procedure, the Power Contributors method has been introduced. According to this method, any cell for any input state can be split up into elementary sub-circuits. By modeling all the leakages flowing onto these sub-circuits, expressions can be derived by just adding each contribution from each sub-circuit. This method has been applied here on an OAI22_X1 complex CMOS cell from NanGate library. Results are promising, since the mean relative error between the derived models and the results from HSPICE simulations is less than 1%.**

Keywords*— *Digital circuit modeling, MOS leakage currents, static power consumption, power contributors.

I. INTRODUCTION

CMOS leakage currents and static power consumption are the key aspects of every low power monolithic digital design. The designer has to take these two quantities into consideration early in the design process, as they are comparable to their dynamic counterparts.

Any circuit library that is going to be used for low power design has to be evaluated in terms of static leakage currents and static power consumption. It is a very time consuming task, since the leakage currents depend on many parameters. First, they are state-dependent quantities for each cell. Different input patterns give different leakage currents and obviously different power consumption. Moreover, these currents depend on the process parameters, the geometry of the transistors, the power supply voltage and the temperature.

In order to facilitate this process, Dhanwada et al [1] introduced the Power Contributors Method, which drastically reduces the modeling effort. Any cell for any input state can be decomposed into smaller and easier to evaluate sub-circuits, the so called Power Contributors (PCs). The leakage phenomena in these elementary circuits can be modeled much easier than in the whole cell. The final expression for leakage current in any cell's terminal can be written as a sum of each Power Contributor's contribution. They appear recurrently in the evaluation process, so they can be used again and again, for different cells and for different input states. This feature makes the evaluation procedure much faster and easier, than modeling each cell for each input combination separately.

In this paper, the method of PCs is applied into a complex CMOS cell, such as a four input Or-And-Invert gate (OAI22), which is designated as OAI22_X1 in the NanGate OpenCell library [2]. The cell is decomposed into PCs and the leakages that flow onto them are modeled by nonlinear regression methods at the Mathematica environment. The provided models are valid for temperatures from 0 to 125^{O}C, for supply voltages in the range of 0.7 to 1.2V and for NMOS transistor widths from 100nm to 415nm. The PMOS transistor width is equal to the NMOS width times 1.5, whereas the transistor length is held constant at L=50 nm. The necessary data for model derivation and validation come from the HSPICE simulator by using the Predictive Transistor Model (PTM) at 45 nm. [3]

II. THE CONCEPT OF POWER CONTRIBUTORS

A. Splitting a library cell in PCs

Suppose that the OAI22_X1 cell is in an input state of A1=0, A2=1, B1=1, B2=0, as presented in Fig.1 (Fig.1)

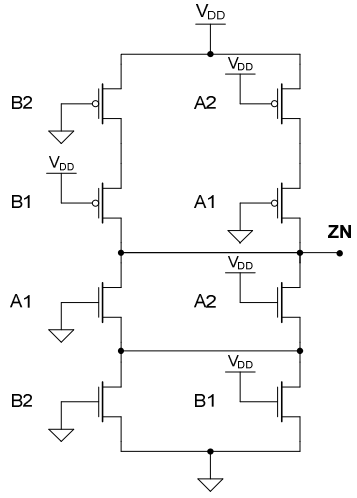

Fig. 1. OAI22_X1 in input state A1A2B1B2="0110".

The first step is the identification of all nodes of the circuit that have a potential almost equal to the power supply (V_{DD}) or ground (GND). These nodes are marked with a "1" or "0" in Fig.2 and they represent the supply or ground potential, respectively. Any MOS transistor or a pair of transistors that lies between these nodes is grouped within a red dashed rectangle.

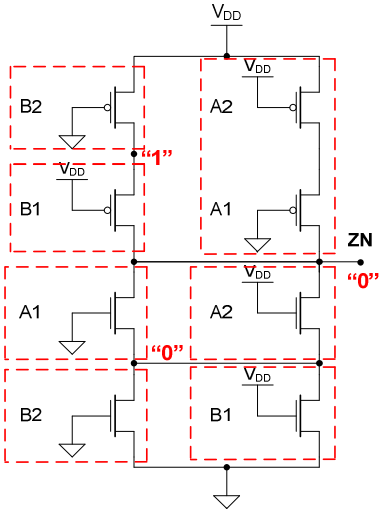

Fig. 2. Identification of nodes with almost-ground ("0") or almost-V_{DD} ("1") potential, and grouping of the transistors between them.

Now, each node with a "0" or "1" designation is connected to a separate ground or V_{DD} terminal, as depicted in Fig 3. The resulting sub-circuits are the Power contributors for this cell in this datum input state (Fig.4).

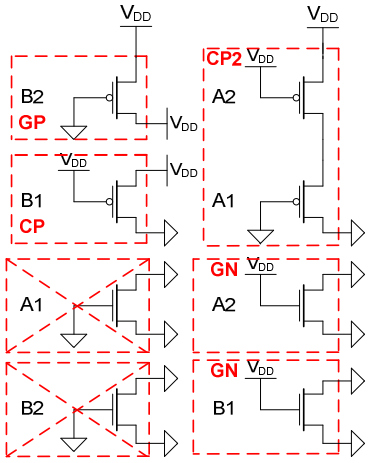

Fig. 3. Connection of the identified nodes in Fig.2 to separate supply – ground terminal. Each rectangle contains a PC.

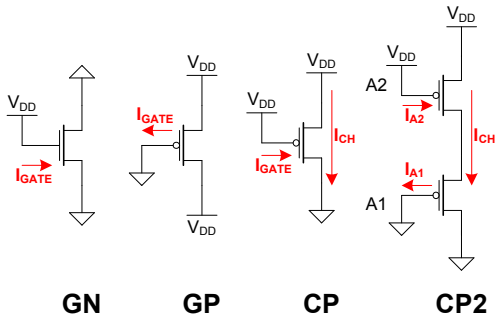

Fig. 4. GN, GP, CP, CP2 PCs from Fig.3. The type and the direction of the leakages is also shown.

The "C" and "G" prefixes, denote the kind of the leakage current that flows on the corresponding PC. A "G" prefix denotes that in the corresponding PC, only gate leakage is present. On the contrary, a "C" prefix denotes the presence of gate and channel leakage flow in the PC. The "P" or "N" suffixes denote that the PC is composed from PMOS or NMOS transistors.

Finally, it is a common situation where some transistors into the red rectangles of Fig.3 to have all its terminals in the same potential. In this situation, there is no current flow into the enclosed transistor, which means that it does not contribute to leakages and two strikethrough lines indicate that it must not be taken into consideration.

B. Deriving the appropriate models for the PCs

The identified PCs of Fig.4 were simulated into HSPICE environment, in order to derive the leakage current values flowing in all of their terminals, for different values of temperature, transistor width and supply voltage. These data were fed into the Mathematica package, in order to fit mathematical models which derive any leakage current as a function of the above sweep variables. These models will be used later to derive the final expressions for the leakage currents in OAI22_X1 cell at Fig.1 and their functional form has as follows:

$$I_{CH}^{CP} = 2.58757\cdot 10^{-11} e^{\frac{-2456.25+(788.781+1.74201(T-1))V}{T-1}} \cdot (T-121.924)(W-6.66929)^{\sqrt{T-1}/V} \quad (1)$$

$$I_{GATE}^{CP} = 3.75468\cdot 10^{-15} e^{-\frac{0.968237}{V}+3.59696V}(W-6.68094)$$

$$I^{GP} = 2.59593\cdot 10^{-19} e^{-4.68241/V+9.55531V} \cdot (T-2744.43)(W-6.66667)V^{-9.5} \quad (2)$$

$$I_{CH}^{CP2} = 1.07738\cdot 10^{-10} e^{\frac{-2491.11+(639.65+0.438293(T-1))V}{T-1}} \cdot (T-1)^{0.46}(W-6.55226)$$

$$I_{A1}^{CP2} = 5.85537\cdot 10^{-20} e^{-0.15110/V+0.546933V} \cdot (T+3685.66)V^{1.58}(W-6.60256) \quad (3)$$

$$I_{A2}^{CP2} = 2.06676\cdot 10^{-15} e^{0.050976/V+2.09504V} \cdot V^{2.09}(W-6.69235)$$

$$I^{GN} = 9.95683\cdot 10^{-16} e^{2.33018V} \cdot (T-1132.68)V^{3.62}(W-9.99702) \quad (4)$$

Units: V[V] (V_{DD}), W[nm] (NMOS), T[K], I[A],

The above models yield a very low error between their predicted values and the corresponding results from HSPICE simulations. For a temperature range of 0^{O}C to 125^{O}C, width of 100nm to 415nm and supply voltage from 0.7V to 1.2V, the mean relative error between Eqs (1) to (4) and HSPICE simulations, does not exceed 1%. In most cases the maximum relative error is less than 2%.

C. Derivation of the leakage models.

The final expression of a leakage current at any terminal is the sum of the particular currents that flow at each corresponding PC. For instance, the leakage current at B2 terminal (Fig. 2) is the gate leakage of GP, whereas the leakage current at B1 terminal is the sum of the gate leakages of GN and CP PCs. Consequently, adding each PC

contribution to the leakage current at any terminal, the expressions below can be derived very easily.

$$
\begin{aligned}
I_{B2} &= I^{GP} \\
I_{B1} &= I^{GN} + I^{CP}_{GATE} \\
I_{A2} &= I^{GN} + I^{CP2}_{A2} \\
I_{A1} &= I^{CP2}_{A1} \\
I_{VDD} &= I^{GP} + I^{CP}_{CH} + I^{CP2}_{CH} + I^{CP2}_{A1} \\
I_{GND} &= I^{CP2}_{CH} + I^{CP2}_{A2} + I^{CP}_{CH} + I^{CP}_{GATE} + 2I^{GN}
\end{aligned}
\tag{5}
$$

The predicted values of Eqs (5) yield a mean relative error of less than 1%, when they are compared with the actual values from HSPICE simulations. This error is comparable with the error that Eqs (1)-(4) yield, when their predicted values were compared with HSPICE simulations. Therefore, it can be stated that the decomposition of the cell into PCs, does not introduce noticeable errors [4].

III. Full Decomposition of Cell OAI22_X1

Following the methodology of the previous paragraph, the OAI22_X1 cell is decomposed into PCs for all its 16 different input states. Each decomposition is depicted in the figures below.

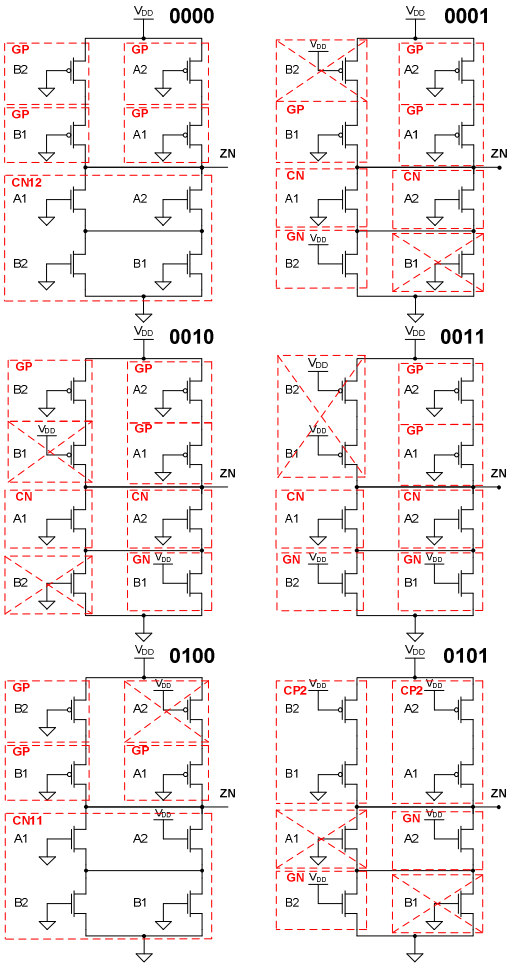

Fig. 5. From top to bottom and left to right: decomposition for input states A1A2B1B2 from "0000" to "0101", respectivelly.

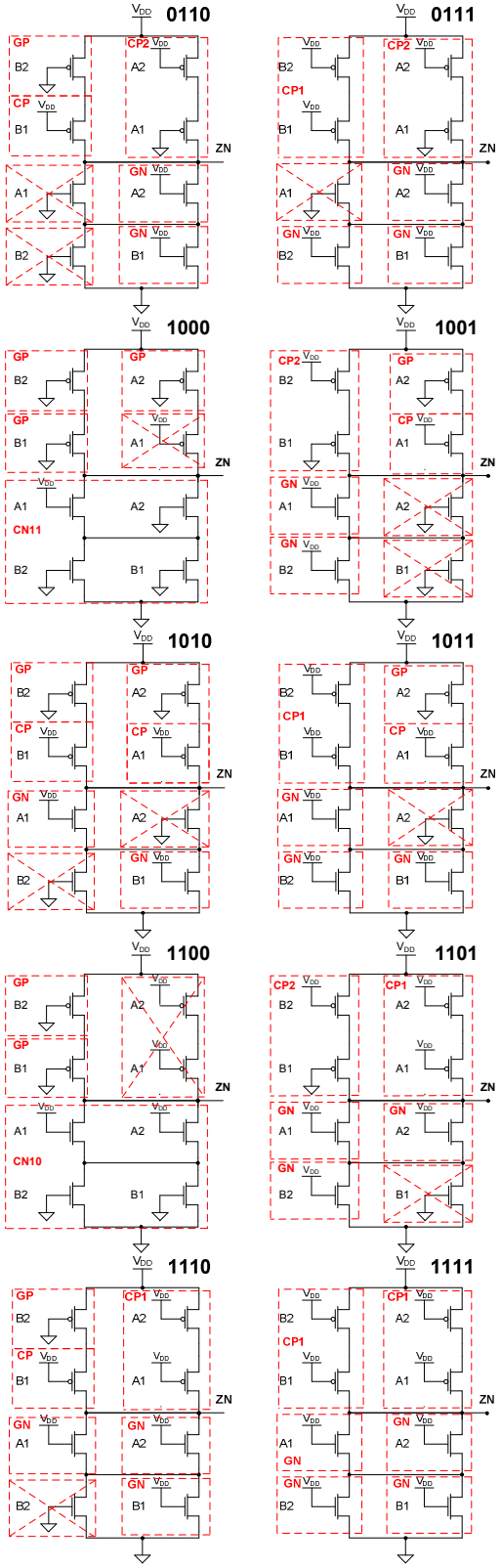

Fig. 6. From top to bottom and left ot right: decomposition for input states A1A2B1B2 from "0110" to "1111", respectivelly.

The current leakages for the above PCs, except from the case of GN, GP, CP, CP2, can be expressed by a set of suitable macromodels, such as:

$$I_{GATE} = c_0(W - W_0)e^{c_1 V + \frac{c_2}{V}} f_1(T) f_2(V) \quad (6)$$

$$I_{CHANNEL} = c_0(W - W_0)e^{\frac{c_1 + (c_2 + c_3 T)V}{T}} g_1(T) g_2(V) \quad (7)$$

The functions f_1, f_2, g_1, g_2 depend on the case, and can take one of the forms below:

$$(x + c_1),\ x^{c_2},\ \frac{c_3 x + c_4}{c_5 x + c_6} \quad (8)$$

ie linear, power or rational function. All these models were fitted within the Mathematica package to the corresponding values from HSPICE and added appropriately in order to produce the final expressions, as in Eqs (5). A comparison between the final expressions and HSPICE results in terms of average relative error lies in Tables 1 and 2. The same comparison in terms of maximum relative error lies in Tables 3 and 4.

TABLE I. AVERAGE RELATIVE ERRORS OF CURRENT LEAKAGES FOR STATES FROM "0000" TO "0111", FOR ALL TERMINALS

	State (A1A2B1B2)							
Terminal	***0000***	***0001***	***0010***	***0011***	***0100***	***0101***	***0110***	***0111***
V_{DD}(%)	0.05	0.13	0.13	0.84	0.84	0.12	0.22	0.21
A1(%)	0.20	0.14	0.14	0.91	0.35	0.22	0.09	0.09
A2(%)	0.20	0.14	0.14	0.39	0.85	0.22	0.35	0.35
B1(%)	0.17	0.14	0.14	0.36	0.36	0.20	0.35	0.35
B2(%)	0.13	0.31	0.56	0.52	0.52	0.22	0.85	0.35
GND(%)	0.25	0.09	0.36	0.09	0.35	0.25	0.25	0.27

TABLE II. AVERAGE RELATIVE ERRORS OF CURRENT LEAKAGES FOR STATES FROM "1000" TO "1111", FOR ALL TERMINALS

	State (A1A2B1B2)							
Terminal	***1000***	***1001***	***1010***	***1011***	***1100***	***1101***	***1110***	***1111***
V_{DD}(%)	0.13	0.22	0.33	0.32	0.15	0.21	0.32	0.40
A1(%)	0.56	0.35	0.35	0.35	0.43	0.35	0.35	0.35
A2(%)	0.31	0.85	0.85	0.85	0.43	0.35	0.35	0.35
B1(%)	0.52	0.09	0.35	0.35	0.32	0.09	0.35	0.35
B2(%)	0.52	0.35	0.85	0.35	0.31	0.35	0.85	0.35
GND(%)	0.22	0.25	0.29	0.29	0.18	0.27	0.29	0.32

TABLE III. MAXIMUM RELATIVE ERRORS OF LEAKAGE CURRENTS FOR STATES FROM "0000" TO "0111", FOR ALL TERMINALS

	State (A1A2B1B2)							
Terminal	***0000***	***0001***	***0010***	***0011***	***0100***	***0101***	***0110***	***0111***
V_{DD}(%)	0.59	1.17	1.17	1.17	0.84	2.34	0.89	2.20
A1(%)	0.89	0.46	0.46	0.46	1.37	0.30	0.30	0.30
A2(%)	0.89	0.46	0.46	0.46	1.82	1.89	1.89	1.88
B1(%)	2.78	3.11	1.88	1.88	1.74	0.31	1.86	1.86
B2(%)	2.76	1.88	2.79	1.88	1.73	1.87	2.81	1.87
GND(%)	1.12	1.40	1.40	1.44	1.61	1.84	1.24	1.69

TABLE IV. MAXIMUM RELATIVE ERRORS OF LEAKAGE CURRENTS FOR STATES FROM "1000" TO "1111", FOR ALL TERMINALS

	State (A1A2B1B2)							
Terminal	***1000***	***1001***	***1010***	***1011***	***1100***	***1101***	***1110***	***1111***
V_{DD}(%)	0.84	0.89	1.55	1.47	1.14	2.20	1.47	3.64
A1(%)	1.82	1.88	1.88	1.87	1.78	1.87	1.88	1.86
A2(%)	1.37	2.81	2.81	2.81	1.76	1.88	1.89	1.88
B1(%)	1.74	0.31	1.86	1.86	1.49	0.30	1.86	1.86
B2(%)	1.73	1.87	2.81	1.87	1.49	1.87	2.81	1.87
GND(%)	1.61	1.24	1.58	1.54	1.32	1.68	1.55	1.61

Therefore it can be stated that all the leakage currents can be modeled with an average relative error which does not exceed 1%. In most of the cases, the maximum relative error does not exceed 2%.

Finally, according to Figs. 5 to 6, the OAI22_X1 cell collapses into 9 different PCs: GN, GP, CN, CP, CP1, CP2, CN10, CN11 and CN12. These PCs require 27 different models in order to describe any gate or channel leakage that flows on them. On the contrary, a complete characterization of the OAI22_X1 cell, without any systematic method, requires 96 more complicated models. So, at least for the OAI22 cell, the modeling effort has reduced by 71.85%.

IV. CONCLUSION

The method of PCs has applied into an OAI22_X1 cell, and allowed the easily derivation of models, that have less than 1% error when compared to HSPICE. These models hold for a broad range of temperature, (0 to 125^{O}C), power supply voltage from 0.7V to 1.2V and NMOS width from 100 nm to 415 nm. Most of the PCs along with the corresponding models were used more than one time, thus reducing the modeling effort by 71.85%.

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