Validation of the Production-Phase Level-1 Data Driver Cards for the Readout and Trigger System of the ATLAS New Small Wheel Detector

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***Abstract*—In order to benefit from the expected increase in luminosity of the upgraded LHC accelerator, the innermost station in the forward region of the ATLAS Muon Spectrometer will be replaced by the New Small Wheel, (NSW) currently under construction. NSW features two new detector technologies (resistive Micromegas detectors, (MM) and small strip Thin Gap Chambers, (sTGC)) comprising $\sim 2.4 \times 10^6$ readout channels. The large number of readout channels, the high data rates and the harsh conditions, under which the NSW will operate, pose significant challenges to its trigger and data acquisition system. The Level-1 Data Driver Card (L1DDC) boards are part of the on NSW detector electronics and mainly consist of high radiation and magnetic field tolerant custom made ASICs. Three different types of L1DDC boards have been developed; two for the readout chain of the MMs and sTGCs and one for the trigger electronics chain of the sTGCs. Over 97% of the 1184 L1DDC boards (572 for the MM and 612 for the sTGC detector technologies) that have been tested at four testing sites are found to operate according to their specifications.**

***Index Terms*—CERN, LHC, ATLAS Experiment, New Small Wheel (NSW), Micromegas, sTGC, L1DDC, FPGA.**

I. Introduction

In order to increase its scientific discovery potential, the LHC will undergo two upgrades; the first (Phase-I) will be accomplished in 2020 while the second (Phase-II) is foreseen for the time period 2024-2026. To maintain its current excellent performance in the resulting higher data rates and higher background radiation environment compared with the previous LHC runs, the ATLAS experiment must upgrade its detectors and electronics [1]. The most complex and challenging Phase-I Upgrade project of the ATLAS detector focuses on the inner wheel-shaped detection station of its Muon Spectrometer [2] (Small Wheel, SW). Since the detectors of the SW are not designed to handle efficiently high particle rates and the trigger system for muon particles is expected to exceed the available bandwidth, the SW will be replaced by a new detection system, the NSW [3]). The NSW employs two sets of detector technologies: the novel Micromegas (Micro-mesh gaseous structure, MM) [3] and the small strip Thin Gap chambers (sTGC) [3], aiming to improve the trigger performance and to provide precise spatial measurements. The NSW consists of eight Large and eight Small sectors which are wedges of MM and sTGC detectors "packaged" together.

The NSW Trigger and Data Acquisition (TDAQ) system's electronics that reside on the detectors have to meet stringent requirements such as the large number of readout channels ($\sim$ 2.1 M for the MM and $\sim$ 331 k for the sTGC), a time latency of 2.5 μs (for Phase-I) and a high radiation and magnetic field environment. To this end, new electronics were designed and manufactured consisting of custom made boards using mainly radiation tolerant ASICs and a series of continuously improved prototypes underwent through rigorous testing before their mass production.

The L1DDC [4] boards are part of the Trigger and Data Acquisition system of the MM and sTGC detectors. They reside on the detectors and they handle the signals exchanged among the detector's Front-End electronics and the off-detector data acquisition network interface (Front-End LInk eXchange, FELIX) [5], located away from the ATLAS detector. Three types of L1DDC boards have been designed and massively produced; two of them are part of the readout path of the sTGC (sTGC-L1DDC) and MM detectors (MM-L1DDC) and

one is part of the trigger path of the sTGC detectors (RIM-L1DDC). In total, 1056 L1DDC boards will be mounted on the NSW (512 MM, 512 sTGC and 32 RIM L1DDCs).

The following sections is a brief overview of the L1DDC board's functionalities, the main components of each board, the developed firmware and software for the quality control of all three L1DDC types. Finally, in Section V the testing procedure is described and the results of the validation tests for all MM and sTGC-L1DDC boards are summarized.

II. The L1DDC Overview

The L1DDCs are radiation tolerant boards handling the exchange of data between the Front-End boards (FE) and the off-detector FELIX network as shown in Fig. 1. On the front-end side the MM-L1DDC will be connected with eight MM FEs and one ART Data Driver Card (ADDC) board (which is part of the MM trigger chain electronics), the sTGC-L1DDC with three sTGC FEs while the RIM-L1DDC interfaces with the on detector trigger electronics of the sTGC detectors (one PAD trigger and eight router boards) via duplex Electrical serial Links (E-Links) [6]. For the interconnection with the on-detector electronics through the E-links, the L1DDC has 36 pins mini Serial Attached Small Computer System Interface (miniSAS) connectors. The back-end side of all three L1DDC types will communicate with FELIX via bi-directional optical fibres (at a rate of $4.8\,\mathrm{Gb/s}$).

The L1DDC is based mainly on the GigaBit Transceiver project, a set of radiation tolerant ASICs that were designed at CERN. The basic component of the L1DDC is the GigaBit Transceiver (GBTX) [6] which is capable of aggregating up to forty E-Links into a single optical fibre. The supported data rates of the E-links are 80, 160 or $320\,\mathrm{Mb/s}$ and can be set by the configuration registers. Additionally, the GBTX has one extra E-Link at $80\,\mathrm{Mb/s}$ for communication with the Slow Control Adapter (SCA) ASIC [7]. The SCA was designed to extend GBTX's functionality by providing a set of peripheral interfaces such as 16 independent I^2C masters, 31 analogue inputs multiplexed to a 12 bit Analogue to Digital Converter (ADC) and 32 General Purpose Input-Output (GPIO) signal pins.

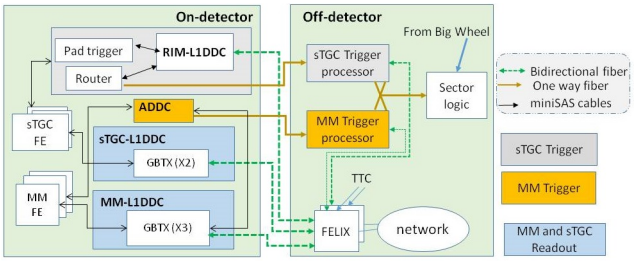

Fig. 1. Block diagram of the NSW trigger and readout electronics chain

A. The MM-L1DDC board

The MM-L1DDC's functionality is to aggregate the readout and monitoring data from the FE boards and transmit them through the optical link to FELIX. Simultaneously, it receives and distributes trigger, timing and configuration data to the FE boards from FELIX.

The MM-L1DDC board's main components are the following radiation tolerant ASICs: the GBTX, the SCA, the FEAST DC-DC converters for the power distribution, the Versatile Transceiver (VTRx) and the Versatile Dual transmitter (VTTx) optical modules used for the interconnection with the FELIX network. The GBTXs are responsible for the multiplexing/demultiplexing of the incoming electrical signals and the distribution of a synchronized clock along with the Timing Trigger and Control (TTC) signals to all on-detector electronics. The SCA handles several actions such as configuration of the GBTXs and environmental variables monitoring such as voltage levels and temperatures via the on-chip ADCs.

The first multifunctional MM-L1DDC prototype board was designed and fabricated in 2014 by the NTUA group hosting one GBTX and also a Field Programmable Gate Array (FPGA) chip for the validation of the proper functionality of the board. Since then, three more upgraded prototypes were developed and all the unnecessary components were removed (FPGA, RJ45 connector, multiplexers port etc.). The L1DDC in order to be compatible with very high particle rates at the High Luminosity LHC and to operate at a first-level trigger rate of $1\,\mathrm{MHz}$, the upgraded MM-L1DDC prototypes feature three GBTxs instead of one. Moreover, the final board is much smaller in dimensions and consumes less energy.

B. The sTGC-L1DDC board

Due to the lower data rate and number of FEs of the sTGC detectors, the space requirements and the specific configuration of the GBTX electrical signals led to the design of a second version of the sTGC-L1DDC. This board consists of two GBTXs and two VTRxs.

The sTGC-L1DDC board has a similar functionality to the MM-L1DDC. Apart from featuring only two GBTX, it hosts two VTRx instead of one VTRx and one VTTx and so their GBTX function both as transceivers. Another important difference from the MM-L1DDC is that this board has less mini-SAS connectors for the interconnection with the FE, so it can only support fewer E-Links. As a result its dimensions are smaller compared to the MM-L1DDC.

C. The RIM-L1DDC board

The RIM-L1DDC interconnects the on-detector sTGC trigger electronics with FELIX. Since only one RIM-L1DDC will be used for each NSW sector, in case of failure, the trigger path of the whole sector will not function. For this reason, the RIM-L1DDC was designed to be redundant and it is separated in two independent and identical parts, the primary part and the auxiliary. Each part of the board consists of one GBTX, one SCA, two VTRXs and three clock fan-out chips. The RIM-L1DDC's functionality is to distribute a) a low jitter $160\,\mathrm{MHz}$ clock to the PAD trigger and router boards, b) $80\,\mathrm{Mb/s}$ configuration and monitoring data, c) TTC data, d)

auxiliary data at $80\,\mathrm{Mb/s}$, e) a synchronous $40\,\mathrm{MHz}$ clock of the LHC proton-proton Bunch Crossing clock and to readout the trigger data.

III. The MM and sTGC L1DDC Quality Control

In order to test the L1DDCs' functionality, a testing setup was assembled using a number of commercial and custom made boards, accompanied by the FPGA firmware and software that was developed for this purpose.

A. The hardware setup

As shown in Fig. 2, the testing setup consists of the following hardware modules; the L1DDC to be tested, one Xilinx VC709 evaluation board, one Texas Instruments CDCE62005 clock generator/jitter cleaner, one custom made FPGA Mezzanine Card (FMC) with nine mini-SAS connectors and a PC. The VC709 evaluation board is a commercial product featuring a Virtex-7 FPGA, one FMC connector and four SFP+ optical transceivers. The three SPFs are used to establish an optical bi-directional link between the L1DDC and the VC709 while the fourth serves as an Ethernet link between the VC709 and the PC. The clock generator is configured to generate and provide to the VC709 a $120\,\mathrm{MHz}$ clock as a reference for the Multi-Gigabit Transceivers (MGT). The FMC board enables the interconnection of the L1DDC's miniSAS connectors with the VC709's FPGA.

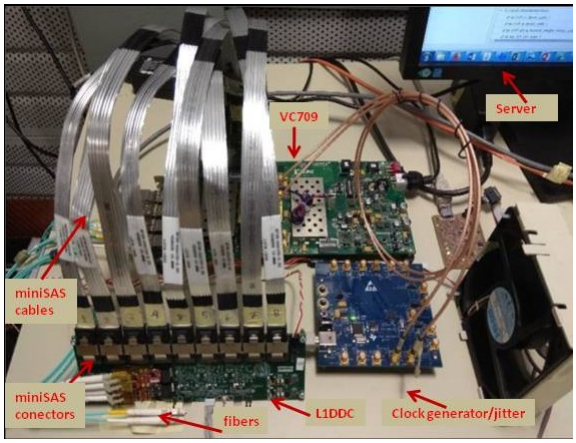

Fig. 2. The L1DDC testing setup.

B. The quality control firmware

Both MM and sTGC final boards were tested extensively using the setup shown in Fig. 3 [4], [8]. The firmware for the quality control tests was based on multiple cores, the GBT-FPGA, the GBT-SC slow control, the Ethernet interface, the Electrical Link Interface (E-Link Interface) and the user logic. The GBT-FPGA is in fact a Multi-Gigabit Transceiver (MGT) that handles the optical links. The GBT-SC and the GBT-FPGA were designed by the GBT team and the later has been modified to handle three optical to emulate the functions of the L1DDC.

The E-Link Interface is the component responsible for the generation, transmission, reception and error checking of the electrical data. It consists of two subsystems, the Transmitter and the Receiver. In the transmitter part, data are generated using the Xilinx®'s Pseudo Random Binary Sequence generator (PRBS). Then, the data are encapsulated with the usage of a Finite-State-Machine (FSM) in a packet of 126 bytes and are transmitted (with the appropriate data rates) to both the E-Links and the GBT-FPGA in order to emulate the data transmission from the FEs and FELIX accordingly. The receiver part is responsible for receiving the incoming data from both the E-links and the GBT-FPGA. For the proper phase alignment of the $320\,\mathrm{Mb/s}$ TTC signals, the Phase Aligner component (utilizing the Xilinx®'s IDELAY primitives) was used in which the signals are properly aligned and forwarded to the Synchronizer. Inside the Synchronizer, the signals are aligned as 8-bit chunks and are forwarded to the Flag detector. The Flag Detector is the sub-component where the packet can be properly detected and the non-data bytes such as the start of packet, end of packet and idle bytes are discarded. The last subsystem of the receiver is the Error Detector where a second PRBS is used to compare the incoming data. For the whole duration of the test a 16-bit counter increments when an error byte is detected.

To complete the quality test of the L1DDCs, the Slow Control (SC) component was also added to the firmware and consists of two parts; the Internal Control (IC) and the External Control (EC). The IC is used to reset and re-configure the GBTX registers with the proper values. The EC is responsible for the communication with the SCA of the L1DDC and the reception of monitoring data (temperatures of the GBTX and FEAST ASICs and voltages of the board). Both IC and EC are communicating with the PC terminal by using an UDP/IP protocols.

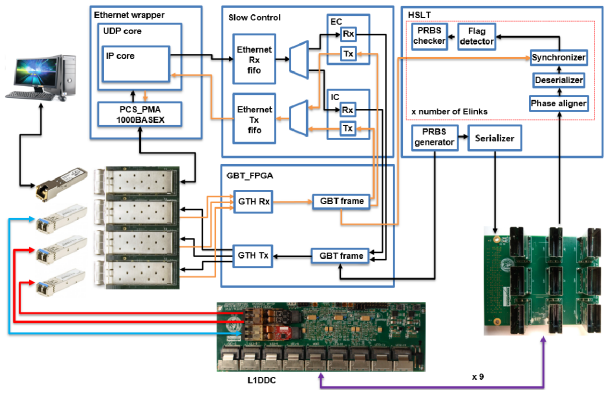

Fig. 3. Block diagram of the firmware implementation.

C. The L1DDC Tester software

To test the large number of L1DDC boards, it was developed, a fully automated, time efficient and user friendly software named L1DDC Tester. The source code was written in C++ programming language and was compiled using the QT Creator Integrated Development Environment (IDE). The working principle of the software is to create requests to the

firmware through a Gigabit Ethernet connection in which the firmware responds with its current parameters. The process of the testing is fully automated and starts by pressing a single button. The first step of the test is to check the optical link stability, then to write/read the configuration registers of the GBTXs in order to verify that the L1DDC's configuration path is functional and that the registers can be accessed. Afterwards, it reads the error counters of the E-Links and of SCA's ADC measurements that include the temperatures of the GBTXs, the temperature of the FEAST DC-DC converters along with their output voltages. The process of reading the error counters and the ADC measurements is repeated every five seconds for half an hour. During that time, if any parameter is above or beyond the specified limits, the test stops with a message showing the name of that parameter. When the testing is completed a log file is generated with the status of the performed tests and the unique IDs of the GBTX and SCA.

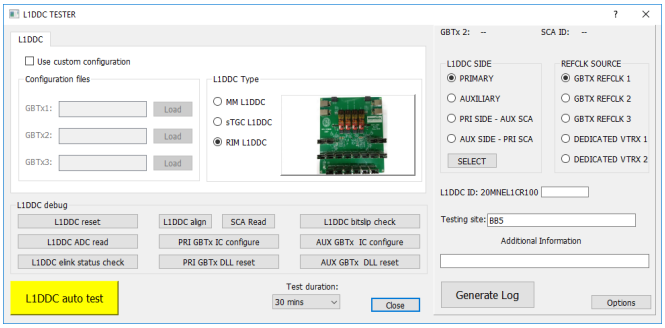

Fig. 4. Software developed for the L1DDC testing procedure.

IV. The RIM-L1DDC Quality Control

The testing scenario of the RIM-L1DDC is different to some extend compared to the other two L1DDCs. Given the different features of the board and the limitations of the existing hardware, a number of modifications are currently carried out in the firmware and the software. The RIM-L1DDC as mentioned before provides to the PAD trigger and routers a 160 MHz clock. For redundancy purposes this clock is generated from five sources. For the primary side of the board the sources are: the primary and the auxiliary dedicated clock VTRXs, two clock outputs from the primary GBTX and one from the auxiliary. The same scheme is also applied to the auxiliary side of the board. The selection of the clock source is done through multiplexers which are controlled by the SCA's GPIO port. The jitter of both GBTX and dedicated clocks was measured with a signal and spectrum analyser to be ~ 4.5 ps and ~ 1 ps respectively. The integrated bandwidth was from 1 kHz to 30 MHz and as a clock source the CDCE62005 clock synthesiser was used.

The firmware and the software of the L1DDC Tester described in the previous sections were modified to test all the clock sources, the fan-out chips that distribute the clocks, the multiplexers, to utilize the GPIO ports of the SCA and to handle the primary and auxiliary parts of the board. Also a phase alignment mechanism was added to the clock receivers of the tester in order to detect glitches to these clocks.

V. Results

The performed tests [9] were able to confirm the bidirectional simultaneous transmission of all electrical and optical signals handled by the L1DDC boards at all supported rates as well as the intended operation of the GBTX, SCA and FEAST ASICs. The initial test was a thermal stress screening with ten cycles and temperatures from 0 °C to 60 °C, an eight hour test to measure the current drain of each individual card and to check if there is any problem with the electrical components. The second phase was a 30 minute test in which the registers of the GBTXs were reconfigured, bidirectional data were transmitted and the constant monitoring of the voltages and the temperatures was performed. Finally, a small sample of boards underwent a 24 hour long test with data transmission. In total 572 MM-L1DDCs, 572 sTGC-L1DDCs and 40 RIM-L1DDCs were tested at four identical test stations implemented at University of West Attica (UNIWA), National Kapodistrian University of Athens (NKUA), National Centre of Scientific Research (NCSR) Demokritos and CERN.

Out of the total L1DDC boards, 32 MM-L1DDC and 35 sTGC-L1DDC failed to pass the tests. So far, nine of the failed MM-L1DDC boards and 22 of the sTGC-L1DDC were repaired and passed the test with a final yield of 97.7% for the MMs, 97.7% for the sTGCs and 100% for the RIM.

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