High performance, wide tuning range 65nm CMOS tunable Voltage Controlled Ring Oscillator up to 11 GHz

Dimitrios Samaras, Alkis Hatzopoulos
Department of Electrical and Computer Engineering
Aristotle University of Thessaloniki
Thessaloniki, Greece
samadimi91@gmail.com, alkis@eng.auth.gr

***Abstract*—This work proposes a novel tunable Voltage Control Ring Oscillator (VCRO), which exhibits high performance in terms of phase noise and wide tuning range. This oscillator is designed to achieve an output frequency range between 2.4 and 11GHz. The proposed oscillator utilizes a band selection technique, in order to maintain an almost constant Kvco equal to 4.6GHz/V. In addition, a current trimming source is used in order to compensate over process and temperature variations. Finally, the oscillator is designed using 65nm CMOS process with a supply voltage of 1V featuring -88.4dBc/Hz phase noise, almost rail-to-rail differential output and 20mA maximum current consumption at 11GHz.**

Keywords— CMOS Ring Oscillators, PLL, VCO, VCRO, TVCRO, Delay Elements, High speed serial interfaces

I. Introduction

Voltage controlled ring oscillators tend to present an attractive solution for implementing high frequency synthesizers over the past years, due to their wide tuning range, simplicity and low die area occupation compared with traditional LC VCOs [1]. One of the most critical parts of frequency synthesizers, PLLs, high-speed communication systems and CDRs (Clock Data Recovery) in terms of noise is the oscillator. The latter should present not only low noise figure but, in addition, low current consumption, wide tuning range, gain linearity over frequency (Kvco) and low footprint. Other choices like LC VCOs can achieve better phase noise than a ring oscillator because of their resonance capability, but they suffer from large area consumption due to the inductor and complexity. Several techniques have been adopted in order to implement a ring oscillator, like current-starved ring oscillators [2], [3], single loop delay cells [4], dual loop delay cells [5], and delay cells using active inductors [6]. In this work, a tunable voltage-controlled ring oscillator (TVCRO) is implemented using 65nm CMOS process, power supply of 1V and frequency tuning range between 2.4 and 11GHz. In Section II, the circuit design of the proposed ring oscillator is introduced and analyzed. In Section III, the simulation results are presented and compared with previous works and Section IV concludes the present paper.

II. Circuit Design

A. Conventional design block

Fig. 1. shows the conventional design block of a single-ended ring oscillator. It is typically consists of an odd number of inverters each one introducing a delay. The loop is intentionally unstable in order to achieve oscillation. Single-ended ROs are suffering from poor common-mode rejection ratio (CMRR) and power-supply noise rejection (PSRR).

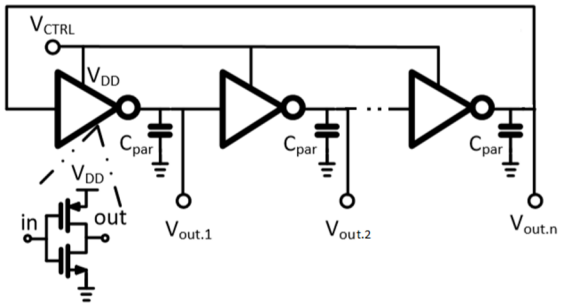

Fig. 1. Single-ended basic topology of a RO

In order to overpass those issues, pseudo-differential delay cells are introduced. Fig. 2. shows a ring oscillator using pseudo-differential delay cells (Fig. 2a), each one contain-ing the blocks of Fig. 2b. That is, a transconductance input stage (g_m), the parasitic capacitance of the output stage (C_{par}), the output conductance g_o of the input stage and the negative conductance g. The negative conductance combined with C_{par} and g_o defines the oscillation frequency. Furthermore, using the equation (1) we can determine the oscillation frequency.

$$f_{osc} = \frac{1}{2NT_d} \quad (1)$$

where N is the number of the delay cells and T_d is the time delay that each cell contributes.

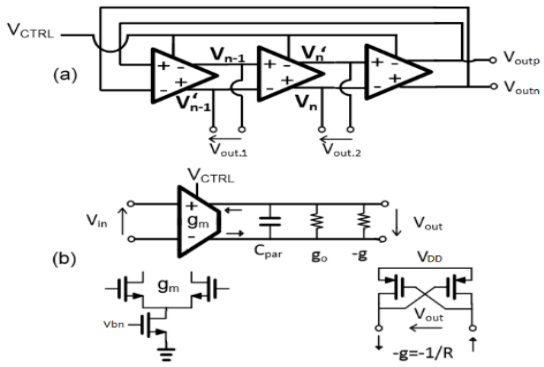

Fig. 2. Pseudo-differential ring oscillator (a). Each cell contains a gm stage and a negative resistance (b)

Apart from the devices presented in Fig.2b, a mechanism that controls the oscillation frequency should exist. In order to utilize that, we inherit the solution presented in [4]. Two pMOS transistors are used in parallel with the negative

resistance. In this work we adopt the architecture presented in Fig. 2a.

B. Circuit implementation

The basic idea of a tunable VCRO is simply by designing two or more VCROs, each one operating in a different frequency band. Depending on the frequency output we would like to synthesize, we select the corresponding VCRO. This architecture offers a K_{VCO} which does not exceed 5GHz/V at all bands. Extremely high K_{VCO} values that traditional VCROs are presenting are difficult to be integrated to a PLL loop which will exhibit a stable performance. The proposed tunable VCRO is presented at Fig. 3. Three VCROs were designed covering the range between 2.4 and 11GHz. Firstly, the "low" VCRO is operating between 2.4 and 6.5GHz. The "medium" VCRO is operating between 6 and 8.6GHz and the "high" VCRO is operating between 8 and 11GHz. Those values were chosen in order to have a relatively good band overlap of roughly 20%. Each VCRO is designed by using three cascaded delay cells as displayed at Fig. 2a. In addition, a multiplexer is designed in order to immune the three VCROs. At Fig. 4. the design of the delay cell is presented. It consists of the input pair, the negative resistance, the current source and two pMOS transistors (hereby called tuners) each one in parallel with the latch pMOS. The control voltage or V_{tune} is connected to the gates of the tuners affecting their transconductance and consequently the current flowing through them. Because of the nature of the pMOS transistors, rising V_{tune} results to lower output current. Frequency and current are proportional and, because of that relationship, the proposed VCRO has a negative K_{VCO}. Each VCRO's delay cell has been designed and sized in order to achieve the frequency range that is desired. Another feature to the proposed VCRO is that the current source can be trimmed during calibration in order to compensate for process and temperature variations.

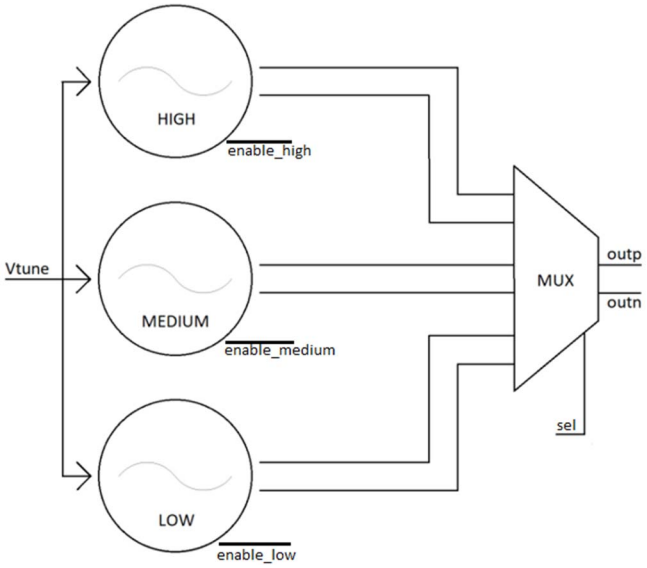

Fig. 3. Top schematic of the tunable VCRO including an output MUX

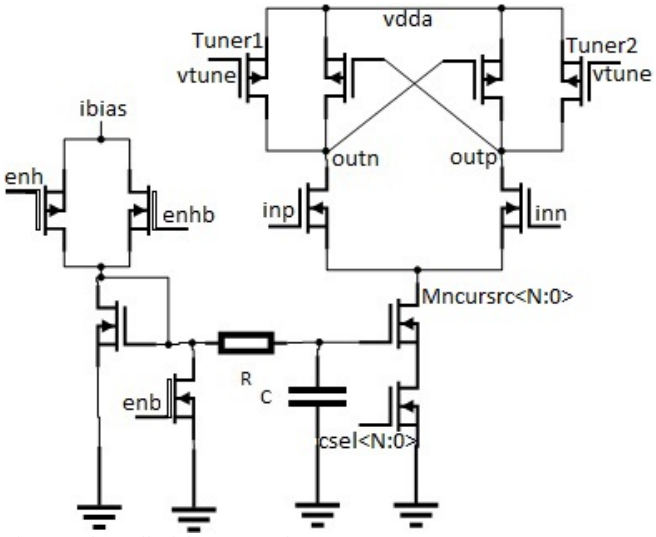

Fig. 4. Delay cell of the proposed VCRO

Each VCRO (low, medium and high) contains three delay cells (Fig.2a). At any time, only one must be enabled in order to avoid kickback noise coming from the MUX. The enable logic is implemented as follows. A transmission gate using thick-oxide devices is used in order to eliminate the current leakage to the ground when the "enb" goes HIGH. Also, a pull-down circuit has been added to the MUX. Bits "enable_high", "enable_medium" and "enable_low" are enabling or disabling the VCROs and at the same time they represent the "sel" bits of the MUX._

In addition, a Low Pass Filter has been added in order to minimize the noise added by the current coming from the current generation circuit (ibias). This results in a better phase noise performance.

The cross-coupled pMOS transistors guarantee the differential operation of the delay cell and define the K_{VCO} in combination with the sizing of the tuners. If the tuners over latch width is rising, then the K_{VCO} is also rising. On the contrary, if this ratio is falling, then the K_{VCO} becomes smaller. Also, tuners and latches must be matched.

Because of the process and temperature variations, ring oscillators suffer from poor frequency stability. Apart from the width of the transistor, the channel length affects the gate-source capacitance (C_{gs}) which plays a decisive role of the time delay and the intrinsic frequency (f_T) that each delay cell is introducing as we can see from equations (2) and (3).

$$C_{gs} = \frac{2WLC_{ox}}{3} + WC_{ov} \quad (2)$$

$$f_T = \frac{g_m}{2\pi C_{gs}} \quad (3)$$

where, C_{ox} is the oxide capacitance and C_{ov} the overlap capacitance. In order to overpass the process variation including the channel length variation, a trimmable current source was designed. Each VCRO has a different programmability. Based on the variation, the current is trimmed and the desired frequency can be achieved. Each VCRO's delay cell was designed using different channel length and current in order to achieve the desired frequency range and K_{VCO}. The lower the channel length, the lower the

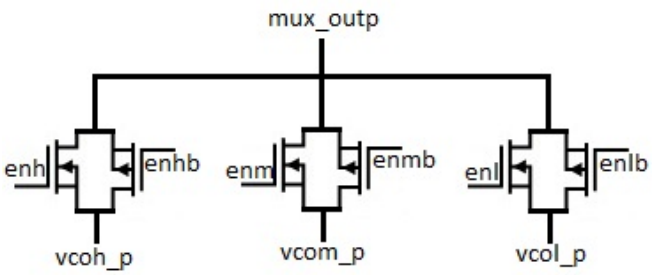

Fig. 5. MUX schematic. Same applies for the negative output

C_{gs} and consequently, the higher the frequency. Finally, the differential MUX is a 3:1. It consists of a pass-gate for each VCRO output. At Figure 5 we can see the schematic for the positive outputs of the three VCROs. The same applies for the negative outputs. The sizing of the pass-gates was optimized in order to have the lowest voltage drop between the drain and the source. Also, the sizing adjustments were optimized for the phase noise performance. The proposed VCRO was designed in order to cover the frequency range desired by a lot of popular protocols. USB 3.1 Gen1, USB 3.1 Gen2, HBR2/3, PCIE GEN3/4, Thunder-bolt 10/20 etc.

III. Simulation Results

In order to validate the theoretical analysis of the proposed VCRO, simulations using Spectre simulator took place. The supply voltage is 1V, and a load of 10fF differentially was used at the output of the MUX. In addition, all the simulations were run at 60 ºC. At Fig. 6. we can see the results of the three VCROs output frequency range over V_{tune}. We can observe that the three VCROs cover the frequency range between 2.4 and 11GHz for V_{tune} values between 100mV and 750mV. The band overlap is at 22.6% between the "high" and the "medium" VCRO and 22.3% between the "medium" and the "low" VCRO. The K_{VCO} for the "high" VCRO is -4.61GHz/V, for the "medium" is -4.1GHz/V and for the "low" is -6.3GHz/V. The K_{VCO} for the "low" VCRO is higher because the range of this VCRO is bigger. At Fig. 7. the outputs of the "high" VCRO at 11GHz are presented. We can see that the output voltage is almost rail-to rail (200mV to 1V). The value of 200mV is because of the current source's V_{ds}. The duty cycle is 46% for the "high" and "medium" VCRO and 50% for the "low". In terms of phase noise, the results are presented at Fig. 8. We can see the phase noise for the three VCROs over V_{tune}. At 11GHz the phase noise is -88.219 dBc/Hz at 1MHz offset.

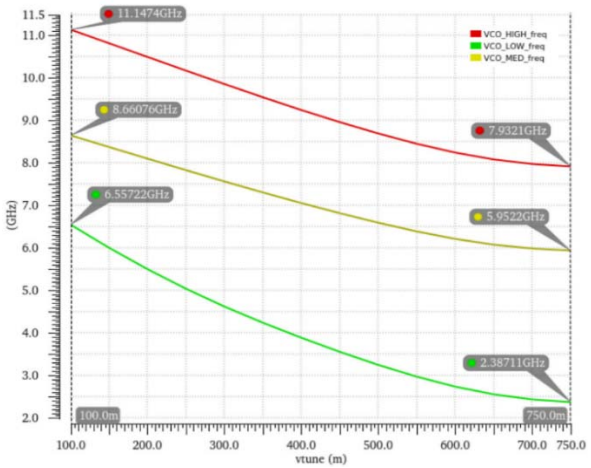

Fig. 6. Frequency range of the three VCROs over Vtune

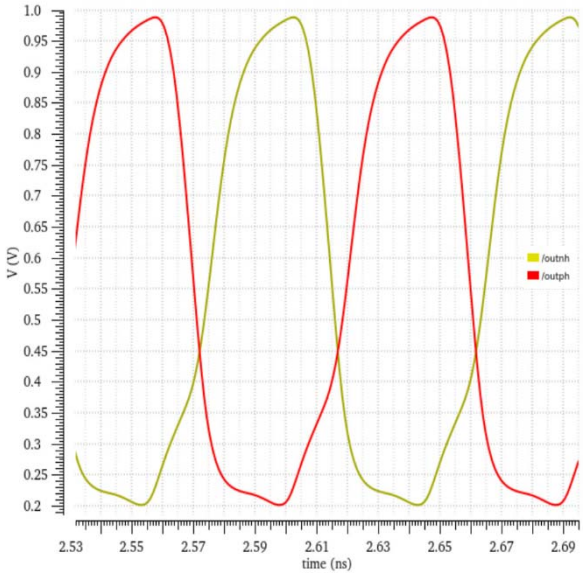

Fig. 7. VCRO "high" outputs at 11GHz

Taking a closer look at the phase noise results, we can see that we can have a better phase noise for a specific frequency using a different VCRO at the overlaps. This is because the main noise contributor at the high frequencies of each VCRO is the tuner pMOS. For example, we can have a phase noise of -94.7dBc/Hz for the frequency of 8GHz using the "high" VCRO and for the same frequency -90.1 dBc/Hz using the "medium" VCRO. The higher the V_{tune}, the lower the phase noise.

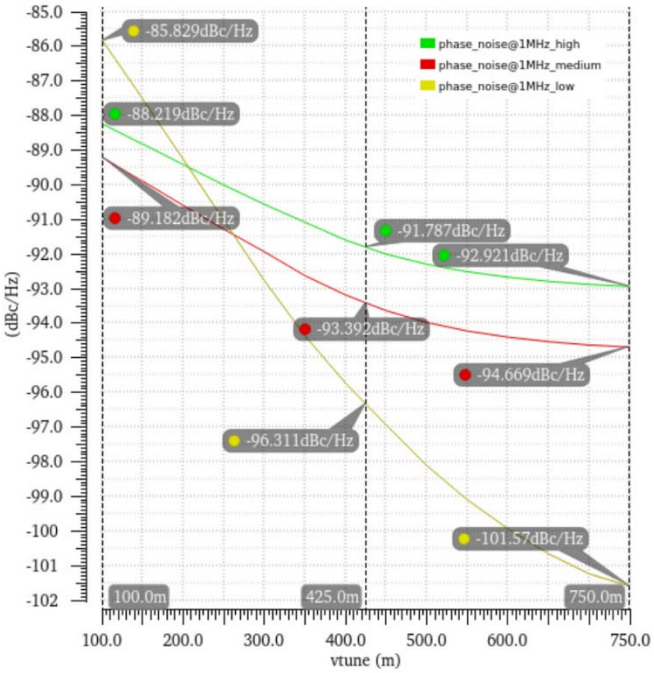

Fig. 8. Phase noise versus Vtune of the three VCROs

The bigger slope of the "low" VCRO is because of the higher gain. Furthermore, at the Table I, we can see the results of phase noise for specific frequencies that popular protocols are using.

TABLE I. PHASE NOISE FOR VARIOUS PROTOCOLS' FREQUENCIES

Protocols	Frequencies and phase noise		
	Frequency	***Phase noise @1MHz offset***	***VCRO enabled***
USB 3.1 Gen1	2.5GHz	-101.1 dBc/Hz	low
HBR2	2.7GHz	-100.2 dBc/Hz	low
PCIE GEN3	4GHz	-95.4 dBc/Hz	low
HBR3	4.05GHz	-95.2 dBc/Hz	low
USB 3.1 Gen2	5GHZ	-91.08 dBc/Hz	low
Thunderbolt10	5.15625GHz	-90.2 dBc/Hz	low
DisplayPort Next Gen	6.75GHz	-93.72 dBc/Hz	med
PCIE GEN4	8GHz	-91dBc/Hz	med
Thunderbolt20	10.3125GHz	-90.08 dBc/Hz	high

In order to compare this work with others, we use figure of merit [11]. The equation is the following:

$$FoM_{db} = L\{f_{offset}\} - 20\log\left(\frac{f_{osc}}{f_{offset}}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right) \quad (4)$$

where $L\{f_{offset}\}$ is the phase noise at the offset frequency, f_{osc} is the operating frequency and P_{diss} is the power dissipation at the operating frequency. At the Table II a comparison between this work and others is presented. The FoM in this work at the oscillation frequency of 10.3125GHz is -157.34 dBc/Hz.

TABLE II. COMPARISON WITH OTHER WORKS

Ref	Performance					
	Freq.	***P.N. @1MHz offset***	***Power***	***FoM (dBc/Hz)***	***Process***	***Supply voltage***
[7]	4.936GHz	-71 dBc/Hz	2mW	-140.96	65nm	1V
[8]	10GHz	-86.2 dBc/Hz	8.2mW	-157.06	40nm	1.1V
[9]	2.3GHz	-108.15 dBc/Hz	65mW	-155.2	0.18um	1.8V
[2]	0.3-2.9GHz	-126.53 dBc/Hz	3.73 mW	-184.97	28nm SOI	1V
[10]	645MHz	-110.8 dBc/Hz	10mW	-157	65nm	1V
This work	2.4-11GHz	-90.08 dBc/Hz	20mW	-157.34	65nm	1V

IV. CONCLUSION

In this paper, a tunable Voltage Controlled Ring oscillator was designed using 65nm CMOS process and a power supply of 1V. The proposed tunable VCRO is able to achieve oscillating frequencies between 2.4 and 11GHz for most of the popular protocols like USB, PCIE, HBR. DisplayPort and Thunderbolt. It presents a phase noise of -90.08 dBc/Hz at 10.3125GHzc, power consumption of 20mW and relatively low K_{VCO} of -4.1, -4.6 and -6.3GHz/V for the "high", "medium" and "low" VCRO respectively. The, comparable with other works, FoM is -157.34 dBc/Hz.

REFERENCES

[1] A. C. Demartinos, A. Tsimpos, S. Vlassis, G. Souliotis, "Delay Elements Suitable for CMOS Ring Oscillators", in Journal of Engineering Science and Technology Review, 2016.

[2] A. Baseer Khan, J. Cardenas, L. Chen, M. Khan, A. Qureshi, "A Low Power and Low Noise Voltage-Controlled Oscillator in 28nm FDSOI Technology for Wireless Communication Applications", in IEEE Canadian Conference of Electrical and Computer Engineering, 2019.

[3] D. Turker, S. Khatri, E. Sanchez-Sinencio, "A DCVSL Delay Cell for Fast Low Power Frequency Synthesis Application" in IEEE Transactions on Circuits and Systems, vol. 58, 2011, pp. 1225–1238.

[4] J. Lee, B. Kim, "A Low-Noise Fast-Lock Phase-Locked Loop with Adaptive Bandwidth Control", in IEEE Journal of Solid-State Circuits, vol. 35, 2000, pp 1137–1144.

[5] I. Kovacs, M. Neag "New dual-loop topology for ring VCOs based on latched delay cells" IEEE, 2018.

[6] E. Sackinger and W. Fischer, "A 3-GHz 32-dB CMOS Limiting amplifier for SONET OC-48 receivers", IEEE J. Solid-State Circuits, vol. 35, no. 12, pp. 1884-1888, 2000.

[7] C. Yen, M. Nasrollahpour and S. Hamedi-hagh "Low-Power and High-Frequency Ring Oscillator Desing in 65nm CMOS Technology", IEEE, 2017.

[8] X. Lin et al. "An 8-11GHz Low Phase Noise Ring Voltage Controlled Oscillator", IEEE International Conference on Electron Devices and Solid-State Circuits, 2017.

[9] R. Rahul, R. Thilagavathy. "A Low Phase Noise CMOS Voltage-Controlled Differential Ring Oscillator", IEEE International Conference on Control, Instrumentation, Communication and Computational Technologies, 2014.

[10] J. Kim, I. Lee, S. Han, S. Lee, "A Low-Noise Four-Stage Voltage-Controlled Ring Oscillator in Deep-Submicrometer CMOS Technology", in IEEE Transactions in Circuit and Systems, Express Briefs, vol. 60, no. 2, pp 71-75, 2013.

[11] P. Kinget, "Integrated GHz Voltage Controlled Oscillators", chapter Analog Circuit Design, W. Sansen, J. H Huijsing, R . J. van de Plassche (eds.) Kluwer Academic Publishers, pp. 353-381, New York : Kluwer Academic Publishers, 1999.