An Alternative Post-bond Testing Method for TSVs

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***Abstract*—Through Silicon Vias (TSVs) are crucial elements for the reliable operation and the yield of three-dimensional integrated circuits (3D ICs). Defects are a serious concern in TSV structures. An improvement of a post bond testing method for TSVs that is based on half Schmitt trigger structures instead of unbalanced inverters is proposed in this work. This method is also used for the detection of short defects, in addition to resistive open ones. Extensive typical model simulations and Monte-Carlo analysis results, using the 65nm technology of TSMC, prove the effectiveness of the proposed improved scheme, which is performing better in terms of robustness and tolerance.**

Keywords—3D ICs, post bond testing, TSV, Monte-Carlo.

I. Introduction

As the CMOS technology is reaching its physical limits, alternative approaches have been proposed, such as the three-dimensional integrated circuits (3-D ICs). 3D ICs provide faster cycle time and lower power consumption, while the vertical stacks of thinned 2D ICs are interconnected by means of Through-Silicon VIAs (TSVs) [1]. New challenges are provoked as the TSVs' fabrication often add problems that are to be faced to reassure the functionality of the IC [2]. Thermal and mechanical stress on the wafer and improper filling of the TSV tube with the conductor material often result to defects. During the bonding process of the dies of 3D ICs, mechanical stress is applied to the layers and tension is induced in the TSVs, resulting sometimes to cracks on the body of the TSVs [3]. Moreover, impurities in the surrounding oxide of the TSV, formed during the TSV fabrication, may create a conductive path through the oxide to the grounded substrate. Such shorts will result in deterioration of the signal quality [8].

3D ICs should be tested for fabrication deficiencies effects. The TSVs are vulnerable to undergo defects during the manufacturing process, the bonding to the next tier, or in the field of operation [4]. So, TSV testing is performed at different stages of the fabrication process. One stage is the pre-bond test. It is performed before the die bonding and targets defects that are created during the wafer manufacturing, such as incomplete fills [6]. Post-bond test, which can additionally target defects that are created upon the bonding process or due to mechanical or thermal stress, is also of significant importance [7].

In this paper, an alternative post-bond testing method to this proposed in [9] is proposed, where the unbalanced inverters are replaced by half Schmitt trigger inverters. Schmitt trigger inverters have been utilized earlier in [12]. However, in [12] a ring oscillator is formed, and the frequency of the generated signal is used for defect detection, which is a different testing approach, vulnerable to process variations [13]. In our work, testing is based on the duty cycle (not the frequency) of a signal that is propagated through the TSV. The capability of this method to detect short defects, in addition to open ones, is also examined. The rest of the paper is organized as follows. The TSV model and its selected geometry are presented in Section II. Section III presents the existing testing method and its improved version. Section IV concludes this study.

II. Lumped Element Model of a TSV

The lumped element model presented in Fig. 1 describes the electrical behavior of a TSV. Resistive open defects are modeled by a resistance in the middle of the TSV, as shown in Fig. 2(a) [10], whereas its value may vary from tenths of mΩ to several kΩ. Resistive short defects are modeled by a resistance through the insulator of the TSV leading to the ground, as shown in Fig. 2(b), whereas its value may vary from several MΩ to some mΩ.

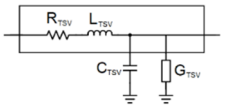


Fig. 1. TSV lumped element model.

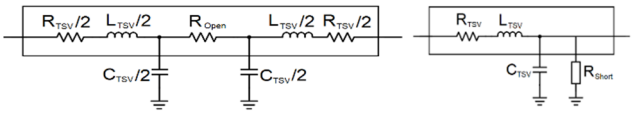


Fig. 2. Electrical Model of a TSV with (a) a void located inside the via and (b) a short through its insulator.

The geometry, materials and fabrication parameters of the TSV are significant for the simulation results, because they alter the values of the TSV lumped element model. The values of the C_{TSV} and L_{TSV} are given in (1) and (2) respectively [11]. For a TSV its height may range from 5μm to above 100μm and its diameter from 1μm to above 10μm, with aspect ratio 20:1 or lower [5]. The adopted parameters of the TSV structure [5] are shown in TABLE I, leading to an approximate R_{TSV}=50mΩ, C_{TSV}=10fF and L_{TSV}=4.5pH. It should be noted that there are more detailed models than this one. However, this is the most commonly used for testing purposes and essential for direct comparison of the proposed scheme with [9]. Due to the large dimensions of a TSV, its process variability is expected to have negligible effect on its performance. So, for the passive elements of the circuitry,

Virtuoso analog library models were used, not any statistical ones. On the contrary, the process variation of all active parts of the circuitry, were considered leveraging TSMC 65nm Monte Carlo models.

$$C_{TSV} = \frac{2\pi\varepsilon_{r,ox}\varepsilon_0 h_{TSV}}{\ln\left(\frac{r_{TSV}+t_{ox}}{r_{TSV}}\right)} \quad (1)$$

$$L_{TSV} = \frac{\mu_0 h_{tsv}}{2\pi}\left[\ln\left(\frac{2h_{tsv}}{r_{TSV}}\right) - \frac{3}{4}\right] \quad (2)$$

TABLE I. PARAMETERS OF THE CONSIDERED TSVs

Parameter	TSV structure simulation values	
	Description	*Value*
h_{TSV}	TSV height	10 μm
r_{TSV}	TSV radius	1 μm
t_{ox}	Insulator thickness	0.25 μm
$\varepsilon_{r,ox}$	Relative permittivity SiO_2	3.9
ε_0	Vacuum permittivity	8.85 10^{-12} F/m
μ_0	Vacuum permeability	4π 10^{-7} H/m

III. Post Bond Testing

A. *Method based on unbalanced inverters*

A representative existing post bond test method, as introduced in [9], from now on called the Unbalanced Inverter Method (UIM), proposes the connection of an unbalanced inverter at the output of the TSV to detect an open defect, as in Fig. 3. The unbalanced behavior of the inverter is a result of a low transition threshold (V_{out_Lth}), or a high one (V_{out_Hth}) by designing the NMOS transistor to be 5 times wider than the PMOS one in the inverter, or vice versa, respectively. The Duty Cycle of the inverter with the V_{out_Lth} (or V_{out_Hth}) is altered proportionally to the size of the open defect that may occur in the TSV. By measuring this Duty Cycle and comparing it to the one of the defect-free case, the defect is detected. Furthermore, for the open defected case, by measuring the difference ΔDC between the Duty Cycles of the High Transition Threshold and the Low one, a greater distinctive ability is achieved. In this paper, the UIM was simulated in Virtuoso, Cadence. The TSMC 65nm technology, the electrical models for the TSV as in Fig. 2 and the parameters for the TSV structure as in Table I were utilized. The PMOS W/L sizing is 120/60 whereas the NMOS one is 600/60. An input voltage pulse of 1GHz was used. The defect-free, the resistive open and the resistive short cases were examined in a Monte Carlo analysis of 500 samples. For the open defected case the Duty Cycle Difference of the V_{out_Hth} from the V_{out_Lth} for the defect-free and the defected case are plotted in Fig. 4 (a) and (b), respectively. For the short defected case the Duty Cycle of the V_{out_Lth} for the defect-free and the defected cases are plotted in Fig. 5 (a) and (b), respectively. In this study, the Duty Cycle (DC) is considered as the ratio of the width of the 'high' pulse, measured at 90% of V_{dd}, to the period 1ns of the pulse.

The duty cycle difference of the defect free case has a mean value of 2.9% and the maximum value at the +3σ limit is approximately 3.6% as exhibited in Fig. 4(a). On the other hand, for the resistive open case of R_{open}=3.2kΩ the ΔDC mean value is 4.6% and the -3σ limit is 3.6%, as shown in Fig. 4(b), which means that the two Monte Carlo plots of the resistive open and defect free cases, do not overlap and the Duty Cycle Difference of the resistive open case is significantly different than the one of the defect free case. Furthermore, the maximum value at the +3σ limit of the defect-free case of the Duty Cycle of the low threshold voltage inverter output is 47.2% whereas the minimum value of the -3σ limit of the resistive short case of R_{short}=4.1kΩ is 47.3%, as shown in Fig. 5(a) and Fig. 5(b), respectively, so, the two Monte Carlo plots do not overlap. Thus, this method classifies correctly the case of open defects down to the value of R_{open}=3.2kΩ and the case of the short defects up to the value of R_{short}=4.1kΩ. In case of defects with lower R_{open} or higher R_{short} values, the Monte Carlo curves of the defect-free and the defective case will overlap, meaning that there will be no significant difference between them and so the defective cases may not be flagged.

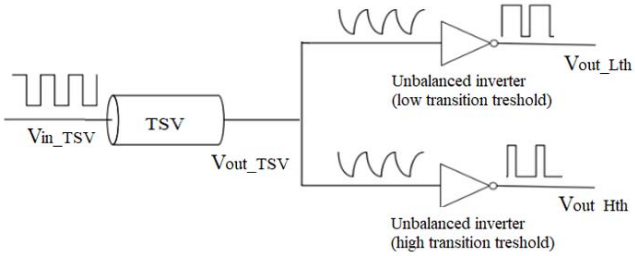
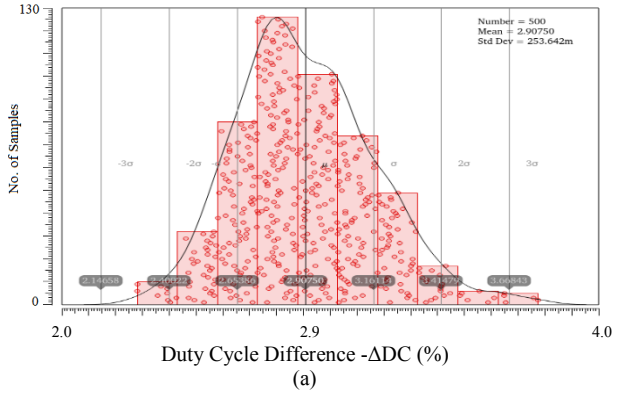
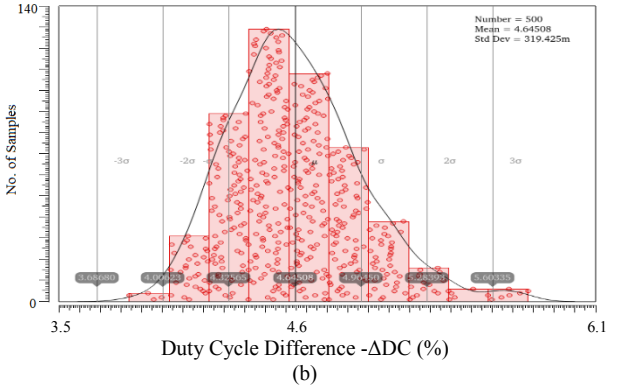


Fig. 3. Unbalanced inverter method scheme.



(a)



(b)

Fig. 4. Monte-Carlo analysis results on the duty cycle difference (ΔDC) for the (a) defect free case and (b) the borderline resistive open defect case with R_{open}=3.2kΩ. Frequency is 1GHz. Number of samples=500.

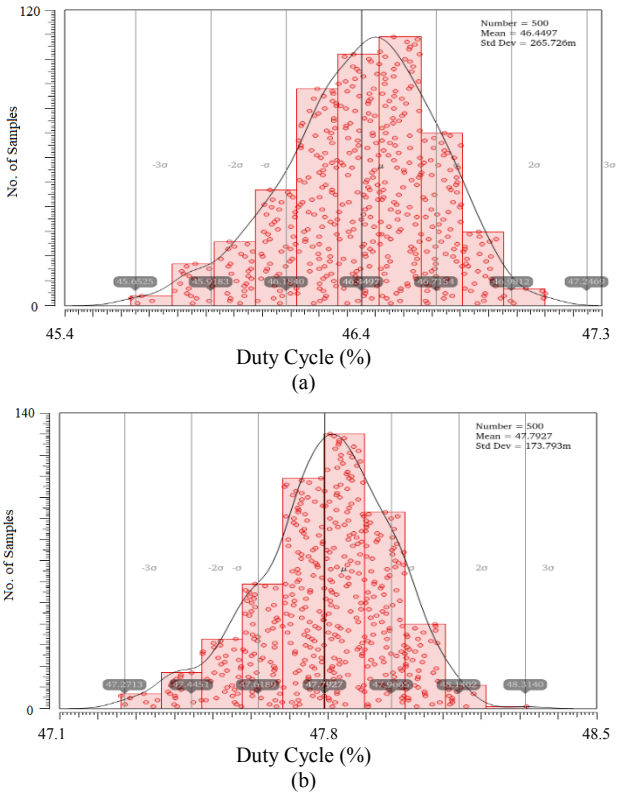


Fig. 5. Monte-Carlo analysis results on the duty cycle (DC) of the low threshold inverter for the (a) defect free case and (b) the borderline resistive short defect case with R_{short}=4.1kΩ. Frequency is 1GHz. Number of samples=500.

B. Method based on Half Schmitt triggers

In this paper, we suggest improving the UIM by replacing the low and high threshold unbalanced inverters with half Schmitt trigger ones, as shown in Fig. 6(a). The half Schmitt trigger inverter schematics are presented in Fig. 6(b) and Fig. 6(c). Again, the Duty Cycle of the V_{out_pmos} and V_{out_nmos} are altered proportionally to the size of the open or short defect that may occur in the TSV. Furthermore, for the open defected case, by measuring the difference ΔDC between the Duty Cycles of the V_{out_pmos} and V_{out_nmos}, a greater distinctive ability is achieved. By measuring this Duty Cycle and comparing it to the one of the defect-free case, the open or short defect is detected.

The proposed method, from now on called the Schmitt Trigger Method (STM), was also simulated in Virtuoso, Cadence. The TSMC 65nm technology, the electrical models for the TSV as in Fig. 2 and the parameters for the TSV structure as in Table I were utilized. In Fig. 6, transistors' sizing is 2W/L=300/60 and W/L=150/60, which results to an area cost comparable to the UIM one. The STM was designed and simulated using again an input voltage pulse of 1GHz. The defect-free, the resistive open and the resistive short cases were tested in a Monte Carlo analysis of 500 samples. For the open defected case the Duty Cycle Difference of the V_{out_pmos} from the V_{out_nmos} for the defect-free and the defective cases are plotted in Fig. 7 (a) and (b), respectively. For the short defective case the Duty Cycle of the V_{out_pmos} for the defect-free and the defective case are plotted in Fig. 8 (a) and (b), respectively.

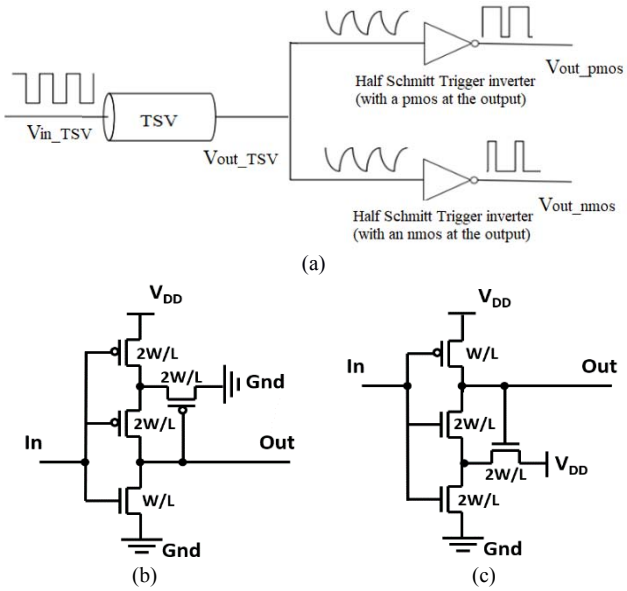


Fig. 6. (a) STM scheme and Half Schmitt trigger schematic (b) with a PMOS at the output and (c) with an NMOS at the output.

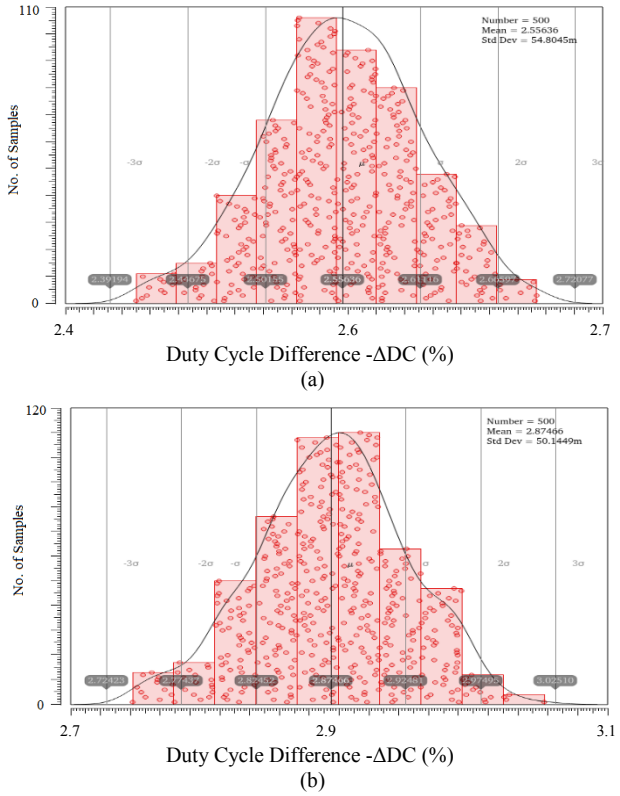


Fig. 7. Monte-Carlo analysis results on the duty cycle difference (ΔDC) for the (a) defect free case and (b) the borderline resistive open defect case with R_{open}=0.4kΩ. Frequency is 1GHz. Number of samples=500.

The duty cycle difference of the defect free case has a mean value of 2.6% and the maximum value at the +3σ limit is approximately 2.7%, as pictured in Fig. 7 (a). On the other hand, for the resistive open case of R_{open}=0.4kΩ the ΔDC mean value is 2.9% and the -3σ limit is 2.7%, as shown in Fig. 7 (b), which means that the two Monte Carlo plots of the resistive open and defect free cases, do not overlap and the

Duty Cycle Difference of the resistive open case is always different than the one of the defect free case. Furthermore, the maximum value at the +3σ limit of the defect-free case of the V_{out_pmos} is 46.7% whereas the minimum value of the -3σ limit of the resistive short case is 46.7%, as in Fig. 8 (a) and (b) respectively, so, the two Monte Carlo plots do not overlap. Thus, this method classifies correctly the case of the open defects down to the value of R_{open}=0.4kΩ and the case of the short defects up to the value of R_{short}=7kΩ.

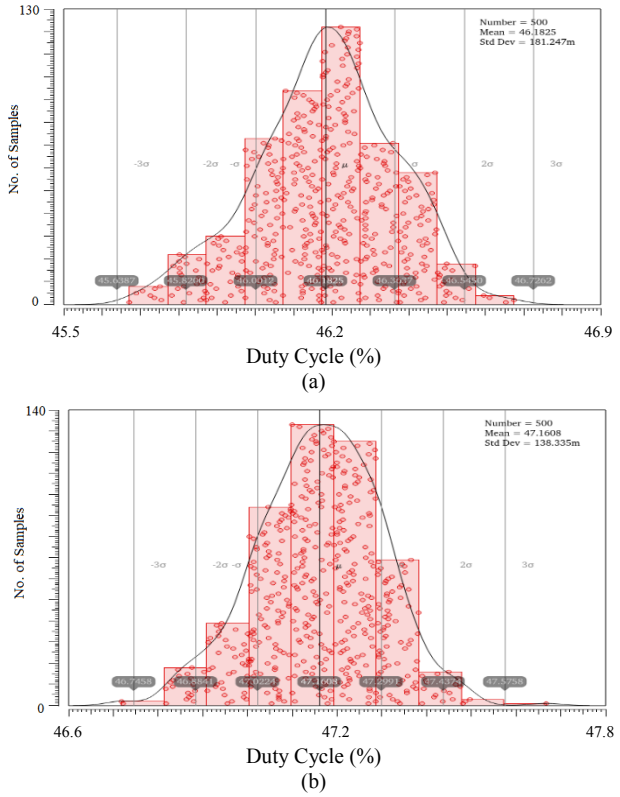


Fig. 8. Monte-Carlo analysis results on the duty cycle (DC) of the pmos-Half Schmitt Trigger for the (a) defect free case and (b) the borderline resistive short defect case with R_{short}=7kΩ. Frequency is 1GHz. Number of samples=500.

C. *Comparisons*

Table III, which presents the comparison of the examined test schemes, illustrates the advantage of our proposed improved Schmitt Trigger Method compared to the original Unbalanced Inverter Method, based on the following criteria. In terms of robustness and tolerance, it detects significantly lower value of R_{open} and significantly higher value of R_{short}, for which the Monte Carlo defective and defect-free curves do not overlap in the range of [-3σ, +3σ]. Also, the proposed method requires about the same cost in silicon area and design effort as the UIM one. Lastly, as the test result is handled by the same circuitry as described in [9], the corresponding area cost of both methods in a real 3D-IC case is the same.

IV. CONCLUSIONS

An improved testing scheme with respect to [9] for detecting defective TSVs is proposed. The proposed STM detects both open and short defects. The Monte-Carlo analysis results, which have been conducted using TSMC 65nm technology models, show that the improved technique is capable to correctly detect defective TSVs for 88% lower values of resistance R_{open} and 71% greater values of resistance R_{short} for the cases of defective TSVs with resistive open and short, respectively. Thus, the proposed scheme performs significantly better in terms of robustness and tolerance in the expense of 45% greater area of the inverters.

TABLE III. Comparison of methods

	UIM [9]	**STM- Proposed in this paper**
Effectiveness	Resistive open & short defects.	
Robustness & tolerance	min R_{open}= 3.2kΩ	min R_{open}= 0.4kΩ
	max R_{short}= 4.1kΩ	max R_{short}= 7kΩ
Inverter Cost Total W of inverters' NMOS & PMOS	1440nm	2100nm
Common Cost of both methods	1 MUX & 1 Transmission Gate per TSV. 23 NOT, 3 NAND, 1 XOR and 3 Counters per 8 TSVs.	

REFERENCES

[1] D. K. Maity, S. K. Roy and C. Giri, "Identification of Faulty TSVs in 3D IC During Pre-Bond Testing," 2018 31st International Conference on VLSI Design and 2018 17th International Conference on Embedded Systems (VLSID), Pune, 2018, pp. 109-114.

[2] J. Jang, M. Cheong and S. Kang, "TSV Repair Architecture for Clustered Faults," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 38, no. 1, pp. 190-194, Jan. 2019.

[3] Y. Yu, X. Fang and X. Peng, "A Post-Bond TSV Test Method Based on RGC Parameters Measurement," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 2, pp. 506-519, Feb. 2020.

[4] Y. Huang, C. Pan, S. Lin and M. Guo, "Machine-Learning Approach in Detection and Classification for Defects in TSV-Based 3-D IC," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 8, no. 4, pp. 699-706, April 2018.

[5] "International Technology Roadmap for Semiconductors", 2013.

[6] F. Ye and K. Chakrabarty, "TSV open defects in 3D integrated circuits: Characterization, test, and optimal spare allocation," DAC Design Automation Conference 2012, San Francisco, CA, 2012, pp. 1024-1030.

[7] A. Hsieh and T. Hwang, "TSV Redundancy: Architecture and Design Issues in 3-D IC," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 20, no. 4, pp. 711-722, April 2012.

[8] X. Fang, Y. Yu and X. Peng, "TSV Prebond Test Method Based on Switched Capacitors," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 1, pp. 205-218, Jan. 2019.

[9] R. Rodríguez-Montañés, D. Arumí and J. Figueras, "Postbond Test of Through-Silicon Vias With Resistive Open Defects," in IEEE Transactions on VLSI Systems, vol. 27, no. 11, pp. 2596-2607, Nov 2019.

[10] G. Katti, M. Stucchi, K. De Meyer and W. Dehaene, "Electrical Modeling and Characterization of Through Silicon via for Three-Dimensional ICs," in IEEE Transactions on Electron Devices, vol. 57, no. 1, pp. 256-262, Jan. 2010.

[11] J. Kim et al., "High-Frequency Scalable Modeling and Analysis of a Differential Signal Through-Silicon Via," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 4, no. 4, pp. 697-707, April 2014.

[12] Y. Lin et al., "Parametric Delay Test of Post-Bond Through-Silicon Vias in 3-D ICs via Variable Output Thresholding Analysis," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 32, no. 5, pp. 737-747, May 2013.

[13] S. Papadopoulos et. al., "Oscillation-based technique for TSV post-bond test considerations," 2017 6th International Conference on Modern Circuits and Systems Technologies, Thessaloniki, 2017, pp. 1-4.