Digital calibration for SAR-CD TDC

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***Abstract*—This paper introduces digital calibration methodology for Time-to-Digital Converters (TDC) based on Successive Approximation Register with Continuous Disassembly (SAR-CD) algorithm. The calibration logic calibrates the internal delays of the circuit to compete against the errors from Process, Voltage or Temperature (PVT) changes. In addition, design enhancements are proposed to optimize for the resources needed for calibration. The results showed enhancements in the Effective Number Of Bits (ENOB) across fabrication and environment corners.**

I. Introduction

In Time-based Analog to Digital Converters (TADC), the conversion is done in two steps. In the first step, the information is converted from voltage change to change in frequency, pulse position or pulse width (time signal). In the second step, this change is resolved to the corresponding digital word. The first operation is performed by the a Voltage to Time Converter (VTC) and the second operation is performed by Time to Digital Converter (TDC), the second block of the full TADC system[**?**].

Low power applications utilizes SAR-based architectures like in [1], [2] and [3]. In each design, one stage is used to resolve all the digital output word bits. This means that any change in the fabrication process or the operation environment can affect the operation of the circuit. To decrease this effect, proper run time calibration should be conducted prior to circuit operation. In [4] and [5], tunable buffers with feedback loop are used to tune the delay between each stage. Error accumulation may need sophisticated calibration effort as in [6].

In [7] and [8], a new algorithm based on successive approximation is introduced. This algorithm moves the conditioning between the evaluated bits in the traditional SAR algorithm to the digital domain. This should decrease the accumulated error processing the algorithm iterations. However, similar to other designs, there are internal delays that should be tuned in a run-time calibration process. An internal delay can be one of two types. The first type is used to achieve synchronization between internal signals to compete the environment effect. The second type represents part of the original algorithm which is generating reference pulses to be compared to the input pulse. In [8], there is one of each type in each stage; one delay to generate the reference signal pulse and another delay to achieve synchronization between the input and the generated pulse.

In this work, a calibration criterion is proposed for the circuit in [8]. The calibration unit should use the same circuit interface as in real operation. Comparison of different operation conditions with, and without, the calibration process is presented in this work.

The rest of the paper is organized as follows. In Section II, the target algorithm is reviewed. In Section III, the target TDC circuit components are reviewed and the main components that need calibration are pointed out. Section IV introduces the main tunable delay circuit and the main design consideration for efficient operation. Section V presents the main calibration logic which uses the same circuit interface to tune the internal delays. Section VI portraits comparison between the original circuit, before and after calibration, for different PVT corner changes.

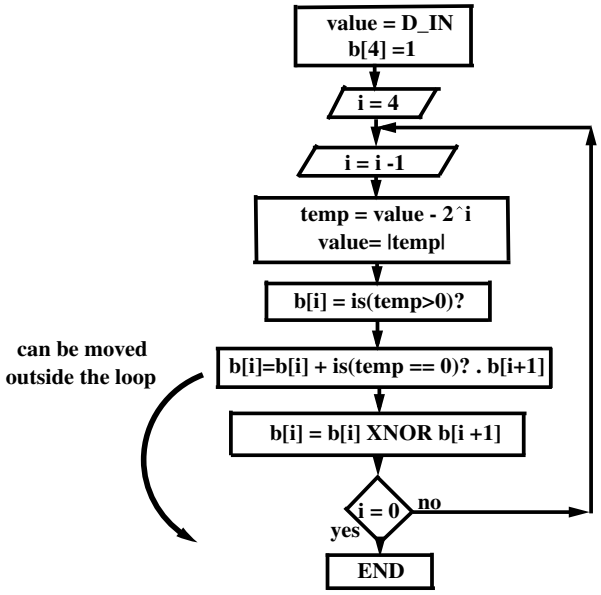

Figure 1. Unit cell of the target system

II. Target Algorithm

Figure 1 shows the algorithm presented in [8]. The flow chart shows an example of converting an analog quantity (D_IN) to the corresponding 4-bits digital representation "b[3] b[2] b[1] b[0]", as 'b[3]' is the MSB and 'b[0]' is the LSB. The local storage element "value" stores the analog input for each iteration and it is updated each iteration. For each iteration, "value" is, first, updated with the absolute difference between the old value and the loop reference weight (2^i). Second, the comparison between the loop input quantity and the loop reference weight decides the iteration un-corrected digital bit. Third, bits correction is applied to the un-corrected bits to produce the final digital bits.

The second and third steps can be performed by digital circuits. As in [8], the comparison is done by a DFF. Also, bits correction, the third step, is a simple digital XNOR operation between the target bit and the bit of the previous iteration. However, performing absolute difference, the first step, requires generation of the reference quantity "2^i". In

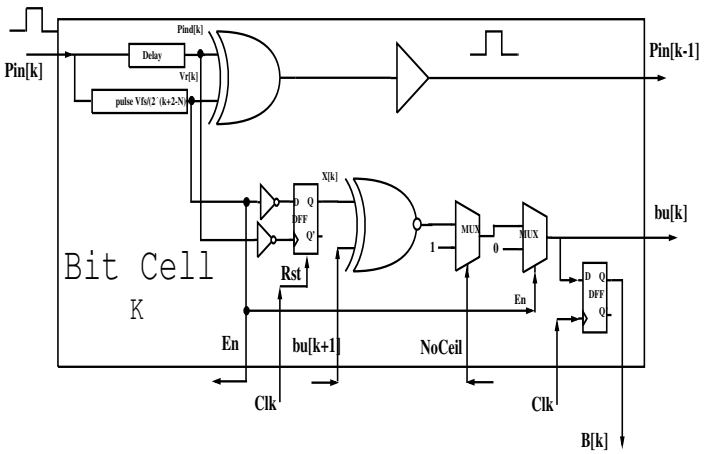

Figure 2. Unit cell of the target system

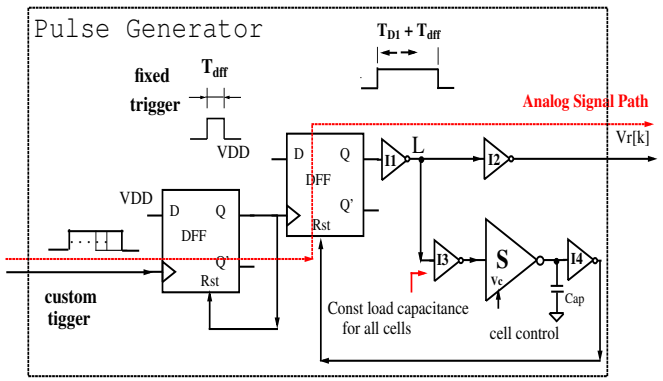

Figure 3. Pulse generator circuit of the target system

the architecture presented in [8], a reference pulse ($V_r[k]$in Figure 2) should be generated for each stage or iteration. The generated pulses should be accurate as it effects the system linearity directly and, hence, run time calibration should be performed for acceptable linearity through normal PVT changes.

III. Target Circuit Components

Figure 2 presents the main unit cell of the target system (Figure 5 in [8]) for a general k'th stage. As mentioned in [8], The input pulse Pin is used to trigger a pulse generator to generate the reference pulse with the corresponding weight. The length of the generated pulse "Vr[k]" is compared to a delayed version of the input "Pind[k]" using the XOR gate to pass the absolute difference to the next stage.The two inputs of the XOR gate should be synchronized for proper operation, hence the delay "Delay" is used to compensate for the pulse generator delay . Changes in the fabrication process and/or the temperature are expected to change this delay and, hence, degrade the system performance. Figure 7 in [8] shows the delay "D1" which is used to control the reference pulse. It is important to calibrate this delay in operation to compensate for PVT changes. The calibration should target both delays; "Delay" and "D1".

Figure 3 depicts a modified version of the pulse generator presented in [8], [9]. The proposed main delay element is a current-starved inverter followed by a small capacitor. The current starved inverted used is portrayed in Figure 4 . Transistors M3 and M4 are small to ensure the inverter operates with very low values of the control voltage "Vc". Vc controls the inverter current driving the load capacitor CL through M5, M6 and the current mirror formed by M7 and M8. Using delays based on capacitor charging results in good dynamic range with low power consumption. However, using large capacitors may decrease minimum pulse width that can be generated. The designer may use one or two delay elements with small capacitors to achieve both high dynamic range with good pulse resolution. The calibration circuit should tune Vc for the best accurate output in the operation environment.

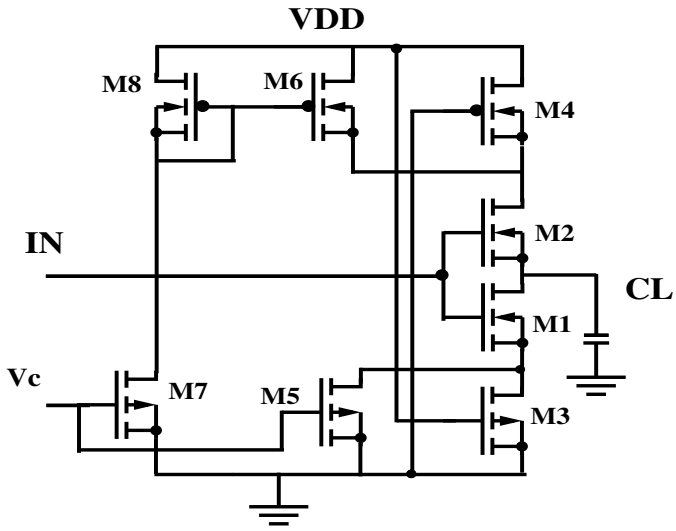

Figure 4. Delay unit consits of current starved inverter followed by loading capacitor

IV. Calibration Algorithm

The calibration logic should tune the pulse synchronization and the pulse generator delays in Figure 2 for proper operation. The calibration of the pulse generation delays is first introduced. Calibration of the synchronization delay follows the same manner and is described after.

Figure 5 depicts the calibration circuit connection diagram. The whole connection consists of: 1-The target SAR_TDC circuit, 2-The calibration logic, 3- The VTC circuit and, 4-A multiplexer (2*1). The multiplexer chooses between either the circuit external input voltage or the calibration circuit input. The VTC converts the chosen input voltage to the TDC input shap as a modulated pulse. The VTC used here is an ideal component which should be replaced with real one in a complete ADC circuit. The target SAR-CD TDC circuit converts the selected input pulse width to the corresponding N-bit digital form (Out[N-1:0]), as N is the number of the

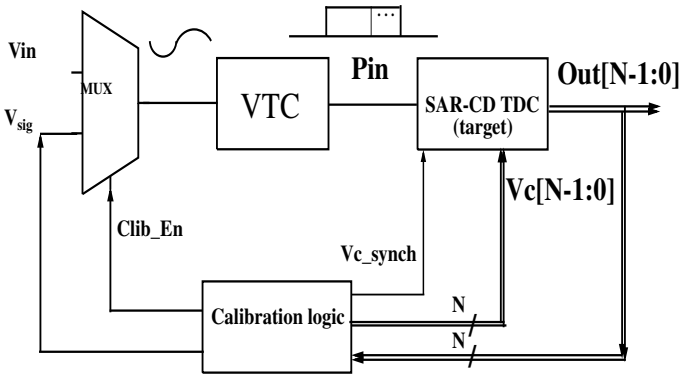

Figure 5. Calibration circuit connection diagram

ADC bits. The calibration logic controls the delay of the pulse generator in each stage (through Vc in Figure 3) to tune the reference pulses generated. This is presented by VC[N-1:0] in Figure 5. The calibration logic also tune the current starved inverter used in signal synchronization ("Vc_synch").

Calibration delay tuning should be performed to Vc signal for each delay. Although there are 2 analog controls needed for each stage with total of 2*N bins, the structure properties for the delay pulse generator features almost constant signal propagation delay across all the stages. This shows the need for only one control bin for all the synchronization delays ("Delay" in Figure 3) (assuming all the remaining circuit components are identical for all the stages). In Figure 3, the signal traveling through the circuit will always see the same path with the same loading. This is achieved by isolating the main current starved inverter "S" and the loading capacitor from the signal path through "I1" and "I3" inverters, which have the same size for all stages. Different pulse widths are achieved by controling "Vc" voltage inverster "S" and using different base loading capacitor for each stage.

Figure 6 portrays the main algorithm for the pulse generator calibration using the analog control voltage Vc[N-1:0], as Vc[N-1] is the analog control voltage for the pulse generator of the first stage which should produce a pulse of half the full scale-width. The control signal ranges from 0.65:1.2V ("Vcfs")."Vsigfs" is the input signal "Vsig" full scale range. It ranges from 0.4:0.6V in this simulation environment. The algorithm logic tests the digital output "Out[N-1:0]" while changing the corresponding Vc[bitAdc], as "bitAdc" is the index of the stage currently being calibrated. "Vcfs" is quantized into 256 level and is presented in 8 bits. "bitCalib" presents the current calibration bit index inside Vc[bitAdc] word. The algorithm loops 8*N times to selects each bit in each control voltage evaluated.

The algorithm starts by assigning Vc[N-1] and Vsig the middle of the control voltage and the input dynamic range respectively. The main loop of the algorithm loops over Vc[N-1] by updating its value in a binary fashion. The update direction, increasing or decreasing, depends on the corresponding monitored Out[N-1] bit. If Out[N-1] is logic 1 ("Out[bit_adc]>0.5?"), then the generated reference pulse

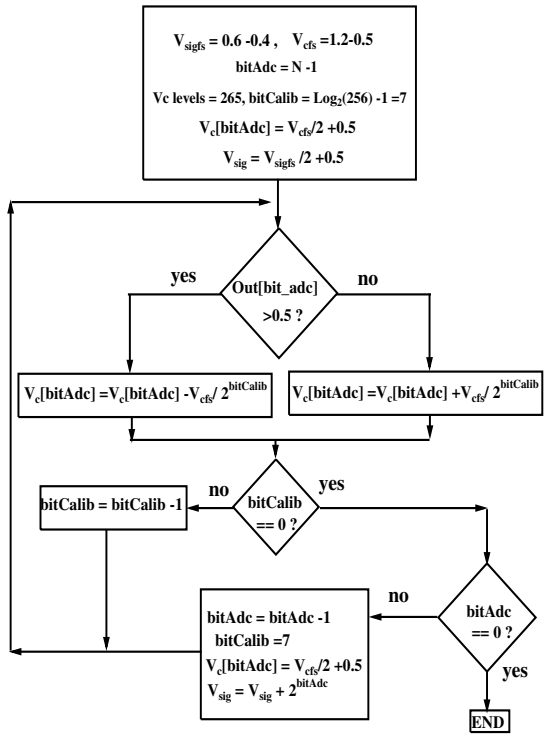

Figure 6. Calibration algorithm diagram

width (Vr[N-1] in figure 2) of the first stage is shorter than the corresponding input pulse width (Pind[N-1] in figure 2), as the later one corresponds to half the full scale. Hence, Vc[N-1] should be decreased to make the generated reference pulse longer. When the algorithm finishes the Vc[N-1] calibration ("bitCalib == 0" is true), the algorithm starts Vc[N-2] calibration (next MSB), by decreasing "bitAdc" and re-initializing "bitCalib" to 7 and starts Vc[N-2] calibration in the same manner.

In this version of the algorithm, the control voltage is quantized into 2^8 levels by initializing "bitCalib" to 7. The designer may increase the voltage resolution more by increasing the initialization value of "bitCalib". The TDC circuit calibration ends when both "bitAdc" and "bitCalib" are zero. Calibrating the synchronization delays, through VC_synch, almost follows the same manner. This is done by loading the maximum input voltage (Vsig maximum) and Vc_synch is tuned for maximum digital output "Out[N-1:0]".

Figure7 shows the simulation graphs of the first MSB, bit '7', calibration. For a full scale time of 31.5ns (check the simulation results section for the rest of the simulation parameters), the first MSB stage reference pulse should be adjusted to a length of 15.75ns (31.5/2 ns). The graph shows the trials of the calibration algorithm to reach the desired value using the feedback signal "Out[7]". As long as Out[7] signal is high, the calibration algorithm controls the reference pulse width through the Vc[7] signal (not shown for clarity) in the direction which increases Vr[7] as spotted in Figure 5. Similarly, when Out[7] signal is low, the calibration logic

reduces Vr[7] signal with the same manner. Figure 5 shows that the calibration is done after evaluating Vc[7] which adjusts Vr[7] as close as to 15.75ns. The resolution of the Vc[7:0] is defined by the designer and should allow a Vr resolution as low as LSB/2.

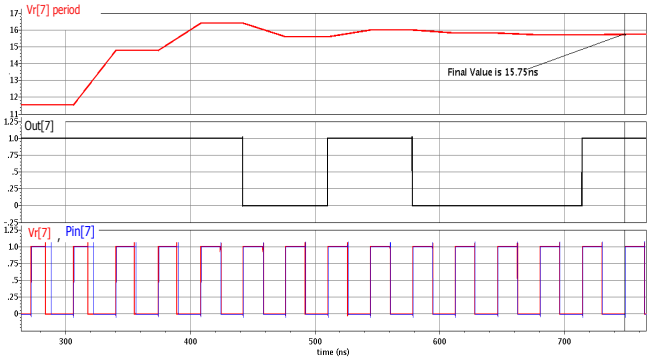

Figure 7. Simulation graphs for first MSB Calibration

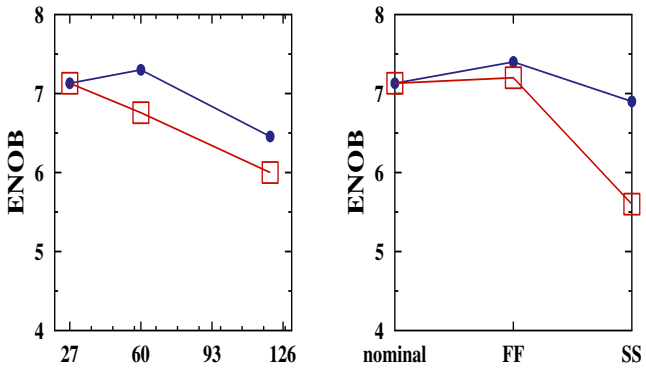

Figure 8. ENOB for the original circuit before calibration (square marker) and after calibration (dot marker). Simulation is for different temperature degrees (left) and different fabrication corners (right)

V. Calibration Results

The calibration enhancement to the circuit is shown by the Effective Number Of Bits (ENOB), as a measure for the system SQNR. The target circuit is a 9-bit version of the one presented in [8]. With the same input setup parameters presented. The input sine wave is of frequency 1.75MHz and is sampled at 29.4 MHz (34ns sampling period). The signal is converted using an ideal VTC to a pulse width-modulated signal with 31.5ns full scale time range. The input signal ranges from 0.4:0.6V. The circuit is tested for different operation temperatures and fabrication corners.

The left graph of Figure 8 shows ENOB values for 27, 60 and 120 Celsius degrees. As the circuit is designed for 27 degree, increasing the temperature changes the internal propagation delays of the circuit and, hence, degrades the circuit performance. At 60 degree, simulation results showed the calibration enhanced the ENOB value from 6.7 to 7.3. The right graph of Figure 8shows system performance enhancement for different fabrication corners; nominal, Fast-Fast (FF) and Slow-Slow (SS).

VI. Conclusion

The calibration logic presented in this work enhances the TADC system linearity for different operation environments. Current-starved inverters can be used to generate pulses of different width with high resolution. The calibration algorithm calibrates the internal delays of the circuit by controlling the current flow in these inverters. The results showed enhancements in the system linearity with different temperatures and fabrication corners.

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